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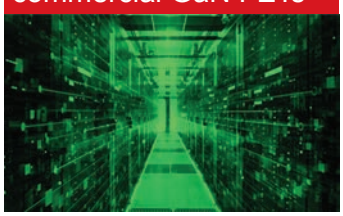
A hike in aluminium improves the GaN HEMT

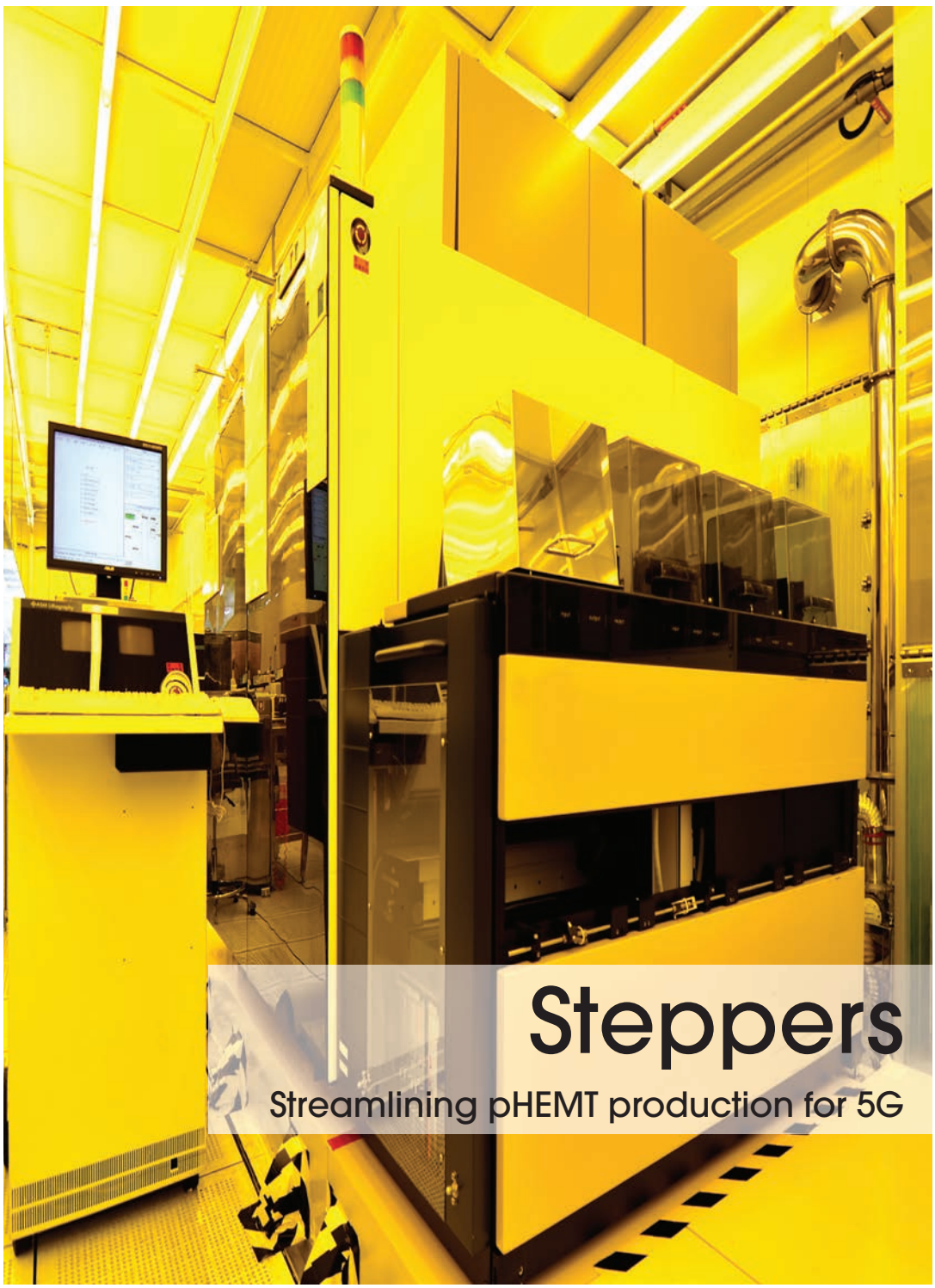
InP HBTs: A candidate for millimetre-wave 5G

Extending the reach of power-over-fibre systems

Obliterating the thermal barrier in GaN-on-GaN

Different face will speed commercial GaN FETs





Steppers

Streamlining pHEMT production for 5G

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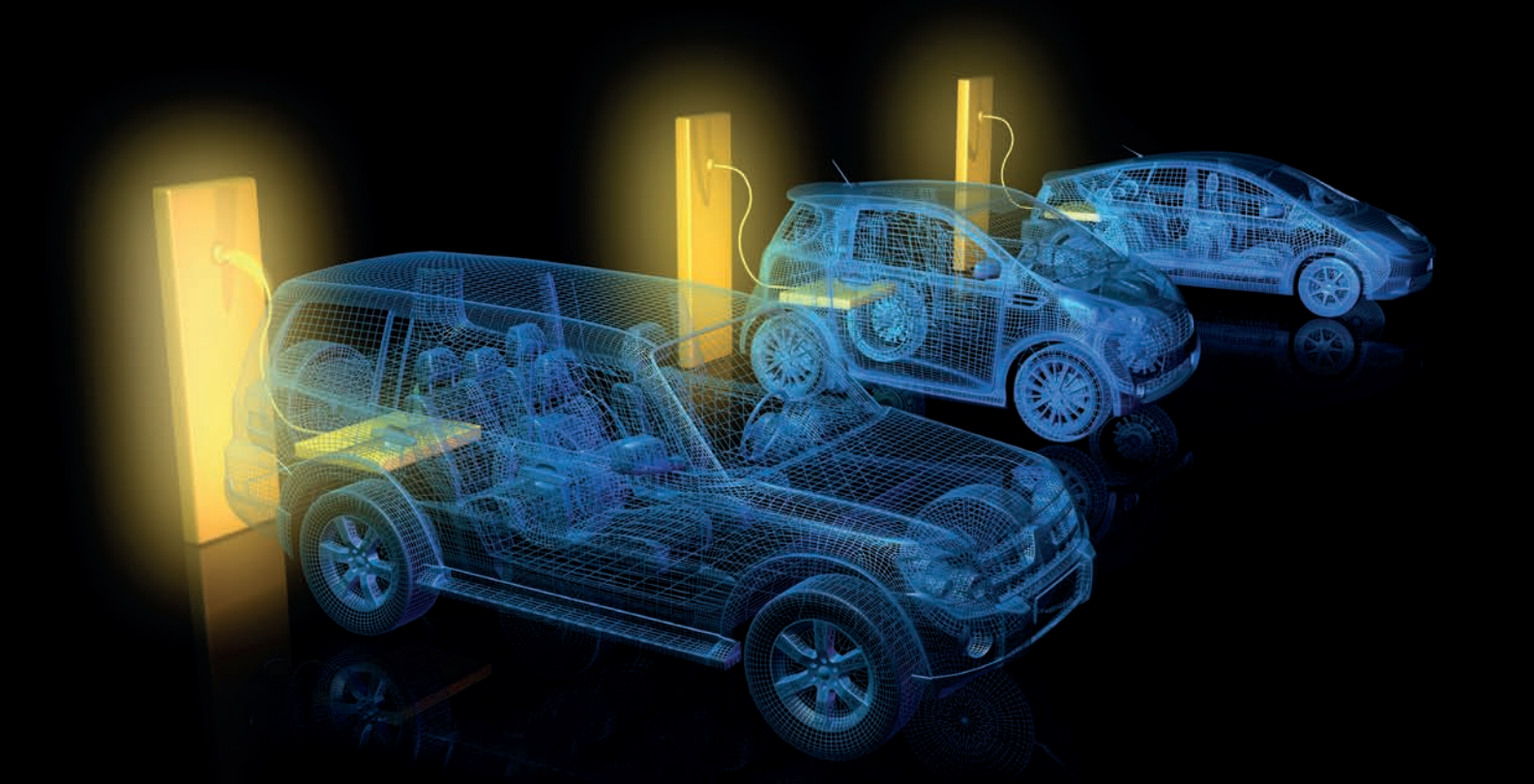

Best performance for next generation SiC power electronics to address global mega trends

AIX G5 WW C

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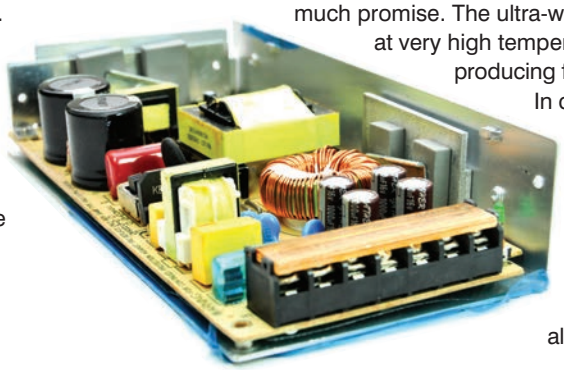
Viewpoint

By Dr Richard Stevenson, Editor

A simpler solution

Our industry is on a journey, trimming carbon footprints by increasing the efficiency of the active components in electrical circuits. This voyage began by replacing silicon diodes and transistors with those made from SiC and GaN, and it is tipped to end with the deployment of ultra-wide bandgap devices.

For the latter, several options exist: AlN; BN; diamond; and, attracting much attention, gallium oxide. Merits of the latter include a relatively easy process for making large, low-cost native substrates, and a variety of deposition technologies for epilayer growth. But these strengths must be weighed against several weaknesses – the thermal conductivity of gallium oxide is low, and advances in device performance hinge on progress in *p*-type doping and a hike in electron mobility.



Maybe, at least in the short-term, it's easier to work with an existing technology, rather than turn to new one. That's the approach taken by a partnership between researchers at the University of Florida and Sandia National Laboratories. They are developing aluminium-rich AlGaN transistors, an approach that can draw on all of the successes in GaN power device development over the last three decades (see p.46 for details of the team's progress).

Cranking up the aluminium in an AlGaN transistor has a dramatic impact on the device's breakdown voltage. When the aluminium content hits 70 percent, the bandgap widens to 5.7 eV, and the breakdown voltage has the potential to reach 13.4 MV/cm – that's roughly five times the value for SiC and GaN.

The devices produced by the US team are already showing much promise. The ultra-wide bandgap aids performance at very high temperatures, with the team's HEMTs producing full gate modulation at up to 500 °C. In comparison, GaN HEMTs fail to provide a full pinch-off above 300 °C. However, judged in terms of breakdown voltage, there is still much work to do. The team's recent devices can withstand 2.5 MV/cm, a value approaching the SiC limit, but far short of the theoretical limit for an aluminium-rich HEMT.

Obviously, it's not going to be down to just this US team to make a breakthrough on this front – or in all the others areas that will enable this class of device to fulfil its potential. As awareness of its capability grows, more groups will make important contributions, leading to ever more researchers getting involved. This should speed the device along its journey, and ultimately help to usher in the era of the ultra-wide bandgap semiconductor.

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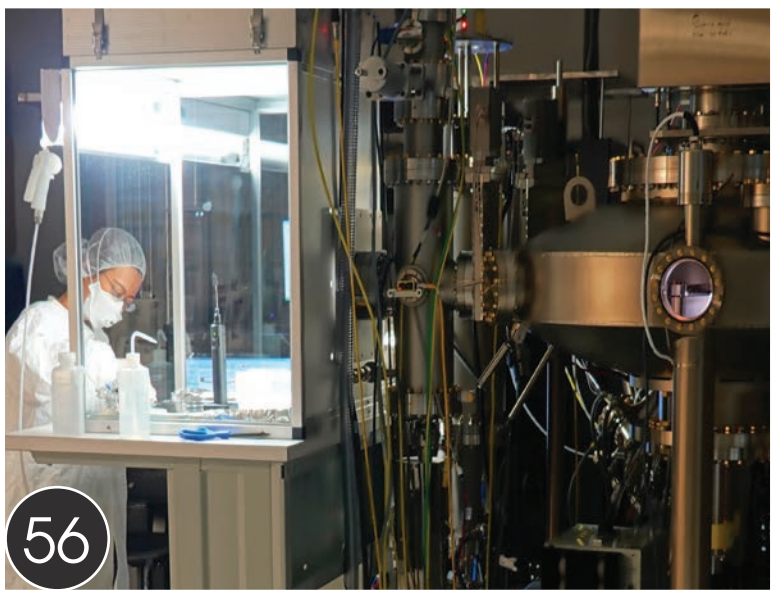

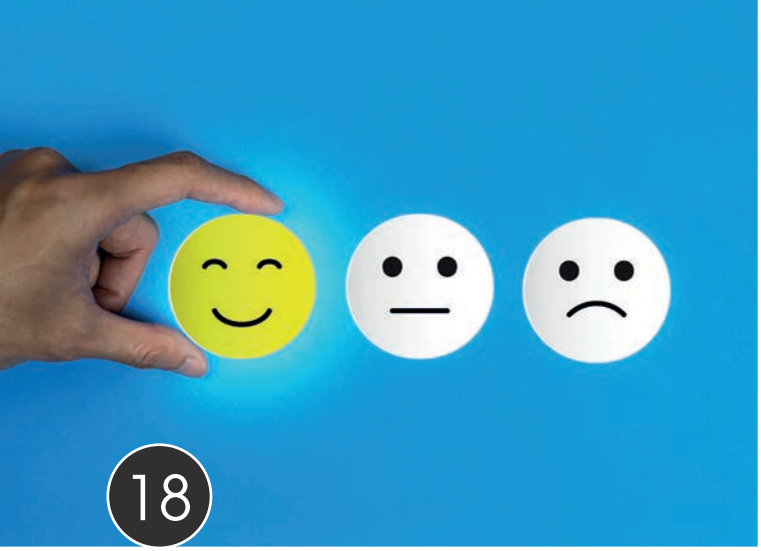

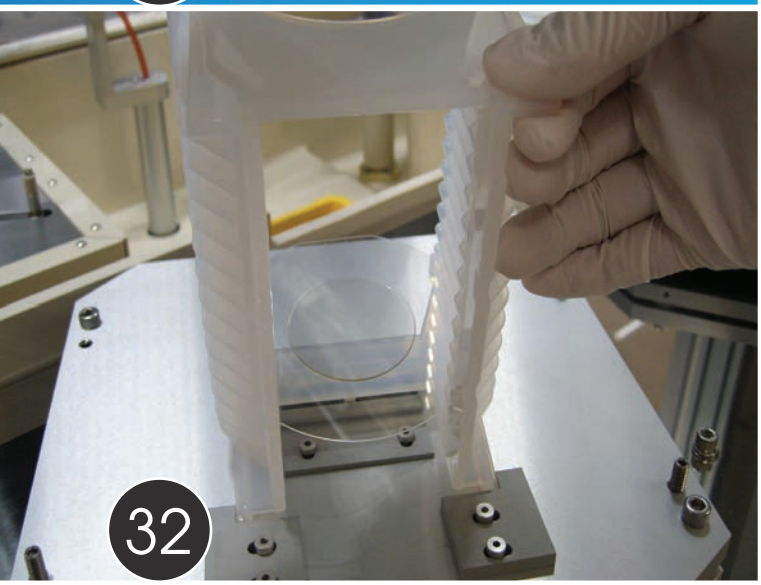

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ST to supply SiC power to Renault-Nissan-Mitsubishi

STMicroelectronics has been chosen to supply high-efficiency SiC power electronics by Renault-Nissan-Mitsubishi (Alliance) for advanced on-board chargers (OBCs) in its upcoming electric vehicles.

Renault-Nissan-Mitsubishi plans to use the new SiC power technology to build more efficient and compact high-power OBCs that will further increase attractiveness of electric vehicles for the users by cutting battery-charging time and enhancing driving range. As Renault-Nissan-Mitsubishi's chosen partner for advanced SiC technology, ST will provide design-in support to help maximise OBC performance and reliability.

ST is also to supply Renault-Nissan-Mitsubishi with associated components, including standard silicon devices. The OBCs with ST's SiC are scheduled to enter volume production in 2021.

EVs need an OBC to handle charging from standard roadside charge points, when a dedicated home-charging system or super-charger is not available. The time to recharge is determined by the OBC power rating. The units in today's EVs have ratings between about 3 kW and 9 kW.

Renault-Nissan-Mitsubishi has already created a 22 kW OBC for the Renault Zoe model, which can fully recharge the battery in about one hour. Now, by upgrading the OBC to SiC power semiconductors (MOSFETs and rectifier diodes), Renault-Nissan-Mitsubishi says it can further reduce the size, weight, and cost while increasing energy efficiency to make future models even more attractive for users and beneficial for the environment.

"As the pioneer and global leader in zero-emission electric vehicles, our objective remains to be the number one provider of mainstream mass-market and affordable EVs around the world," said Philippe Schulz, Alliance VP Design Electric and Hybrid Powertrain. "The small size, light weight, and high energy efficiency we can achieve using ST's SiC technology in our OBC, combined with the increased battery efficiency, will enable us to accelerate the adoption of electric vehicles by reducing charging times and extend the range of our EVs."

Marco Cassis, president, sales, marketing, communications and strategy development, STMicroelectronics, said, "SiC technology can help the world by reducing dependence on fossil fuels and increasing energy efficiency. ST has successfully developed manufacturing processes and established a portfolio of qualified, commercialised SiC products also in automotive-grade version."

"Building on our long cooperation, we are now working with Renault-Nissan-Mitsubishi to realise the many advantages SiC can bring to EVs. Moreover, this commitment helps ensure success by increasing the economies of scale to deliver superior-performing SiC-based circuits and systems that are also cost-effective and affordable."

Qorvo GaN in US army radar system

RF COMPANY Qorvo has announced that one of its GaN power amplifiers has been selected by Lockheed Martin to provide GaN modules for production of the US Army's Q-53 radar system.

Using GaN technology in this multi-mission mobile radar will improve efficiency, power density, reliability and lifecycle cost over the GaAs amplifiers currently used in the system. The S-band MMIC high power amplifier (HPA) is built on Qorvo's GaN-on-SiC technology. The GaN HPA delivers more than twice the saturated output power and a fifteen-point improvement in power-added efficiency (PAE) over the GaAs predecessor.

These capabilities support needed functions of the phased-array Q-53 radar, such as long-range counterfire acquisition. The amplifier's compact size and high performance supports a wide range of challenging operating conditions. GaN-on-SiC technology has the added benefit of increasing system reliability and reducing lifecycle ownership costs.

James Klein, Qorvo's president of infrastructure and defence products, said: "GaN-based amplifiers are providing RF system engineers with the flexibility to achieve significantly higher power and efficiency than GaAs while using fewer parts. The Q-53 radar system exemplifies just how closely Qorvo works with its defence customers to bring commercial technology to military applications that operate across the spectrum with the highest levels of reliability and functionality. We are proud to be selected by Lockheed Martin to help upgrade the US Army's most modern radar system."

Lockheed Martin has used an open GaN foundry model leveraging relationships with commercial suppliers, like Qorvo, that use the power of the expansive telecommunications market. This process takes advantage of the commercial industry's investment in GaN, enables competition and ultimately reduces costs.

Delphi and Cree partner on automotive SiC devices

DELPHI TECHNOLOGIES, a provider of automotive propulsion technologies, and semiconductor firm Cree have announced a partnership to use SiC technology to enable faster, smaller, lighter and more powerful electronic systems for future electric vehicles (EVs).

Cree's SiC-based MOSFET technology will be combined with Delphi Technologies' traction drive inverters, DC/DC converters and chargers to extend driving range and deliver faster charging times of EVs, while also lowering weight, conserving space and reducing cost.

The Cree SiC MOSFETs will initially be used in Delphi Technologies' 800 V inverters for a premium global automaker. The inverters are being designed to provide vehicle engineers with additional flexibility to optimise powertrain systems.

Options include more range or a smaller battery; ultra-fast charging or smaller, lighter, cheaper cables; and greater harvesting of vehicle kinetic energy when braking. Production will ramp in 2022.

"Delphi Technologies is committed to providing pioneering solutions to vehicle manufacturers," said Richard Dauch, CEO of Delphi Technologies.

"Our collaboration with Cree will create a significant benefit to automakers as they work to balance meeting stricter global emissions regulations with consumer appetite for electric vehicles. Overcoming driver anxiety related to electric vehicle range, charging times and cost will be a boon for the industry."

The adoption of SiC-based power solutions is rapidly growing across the automotive market as the industry seeks to accelerate its move from internal combustion engines to EVs.

IHS estimates that, by 2030, 30 million high voltage electrified light vehicles will be sold representing 27 percent of all vehicles sold annually. Inverters are one of the highest-value electrification components and their efficiency has an industry-changing impact on many aspects of vehicle performance.

"Cree's technology is at the heart of the dramatic change underway in EVs, and we are committed to supporting the automotive industry as it transitions from silicon-based designs to more efficient, higher performing SiC solutions," said Gregg Lowe, CEO of Cree.

"This partnership with Delphi Technologies will help drive the adoption of SiC in the automotive sector. Cree is continuing to expand capacity to meet market demands with our industry-leading power MOSFETs to help achieve a new, more efficient future."

Power integrations LED drivers sse PowiGaN technology

POWER INTEGRATIONS has announced new high-power-density members of its LYTSwitch-6 family of safety-isolated LED-driver ICs for smart-lighting applications. The new ICs use PowiGaN technology to enable designs that deliver up to 110 W with 94 percent conversion efficiency using a simple, flexible flyback topology.

The high efficiency of the new LYTSwitch-6 ICs eliminates the need for heatsinks – greatly reducing ballast size, weight and cooling airflow requirements, according to the company. The 750 V PowiGaN primary switches provide low $R_{DS(ON)}$ and reduced switching losses. This improvement, combined with existing LYTSwitch-6 features, increases power conversion efficiency by up to 3 percent compared to conventional solutions – reducing wasted heat by more than one-third.

LYTSwitch-6 ICs with PowiGaN technology employ lossless current sensing, which contributes to the higher efficiency. The new family members retain existing LYTSwitch-6 benefits such as fast transient response, which facilitates excellent cross regulation for parallel LED strings without the need for additional regulator hardware, and flicker-free system operation. This allows simple implementation of a pulse-width-modulation (PWM) dimming interface.

Comments Hubie Notohamiprodjo, director of product marketing for LED lighting at Power Integrations: "The new LYTSwitch-6 ICs with PowiGaN technology enable highly efficient designs up to 110 W for smart residential and commercial fixtures and low-profile ceiling troffers. The high power density of LYTSwitch-6 designs enables reduced height and weight, which is vital for space-constrained and sealed ballast applications."

BluGlass and Bridgelux sign new joint development agreement

AUSTRALIAN semiconductor firm BluGlass has signed a Joint Development Agreement (JDA) with US-based LED company, Bridgelux. The agreement is to develop cascade LEDs using BluGlass' patented remote plasma chemical vapour deposition (RPCVD) technology, to establish a path for mainstream applications in the general lighting market.

BluGlass and Bridgelux will work to develop competitive applications for the growing general lighting market, using BluGlass' RPCVD tunnel junction technology.

For over 15 years, Bridgelux has designed and produced LED lighting solutions for the general lighting market that are high performing, energy efficient, cost-effective and easy to integrate. Bridgelux's focus on technology development has yielded proprietary innovations in LED design and manufacturing processes that enable its products to deliver the right quality of light and accelerate mass adoption of LED lighting.

The joint development program aims to successfully integrate BluGlass and Bridgelux's technologies in high performance commercial LED applications, and drive commercial adoption of RPCVD-enabled cascade LEDs for general lighting through the future provision of RPCVD equipment and process licensing. The terms of the JDA are non-exclusive and will provide revenues to BluGlass for its development work.

BluGlass recently demonstrated an industry breakthrough with its patented 'active as grown' RPCVD tunnel junctions for LED wafers. These tunnel junctions could solve the industry challenge of efficiency droop, by combining multiple LEDs in a single vertical LED stack – generating greater light output for less power.

"Bridgelux is a leader in solid-state lighting innovation and is always working on developing new technologies for the LED lighting industry. We look forward to exploring the potential of RPCVD with BluGlass," said Tim Lester, CEO of Bridgelux.

Giles Bourne, CEO and managing director of BluGlass, said: "We are delighted to have Bridgelux as a development partner to help deliver the competitive advantages of RPCVD tunnel junctions into this important, high-growth market. Bridgelux is an innovative leader, producing premium lighting to high-end markets around the globe. This commercial partnership marks an exciting milestone for BluGlass and we look forward to enabling the lighting technologies of the future together."

Emcore appoints Noel Heiks to board of directors

Emcore has announced the appointment of Noel Heiks to its board of directors.

"We are extremely pleased to have Noel join us," said Gerald Fine, Emcore's chairman of the board.

"Noel's significant experience managing high growth defence and optoelectronics companies positions her well to make valuable contributions to Emcore and our board of directors."

Heiks has extensive executive management and entrepreneurial experience in high-tech companies, including defence and optoelectronics companies.

From March 2018 to April 2019, Heiks served as president and COO of Duos Technologies, a company specialising in AI and machine learning for inspection and security applications. From August 2017 until March 2018, Heiks served as Interim CEO of MVTRAK, an early stage health monitoring company.

In 2008, Heiks founded Nuvotronics, a manufacturer of radar and wireless systems for defence and telecom organisations, serving as its CEO and then board member until its eventual acquisition by Cubic Corporation in March 2019.

In 1996, Heiks founded Haleos, a manufacturer of microfabricated optoelectronics components, and served as its vice president until its eventual acquisition by Rohm & Haas in 2002, where she went on to serve as marketing director of Rohm and Haas (now Dow Chemical) from 2002 until 2007.
Heiks holds a BSc in Physics and an MSc in Electrical Engineering from Virginia Tech University and holds approximately 30 awarded or pending patents.

Eta Research develops polished 100 mm GaN wafers

ETA RESEARCH, a Chinese semiconductor company with headquarters in the new Lingang Free Trade Zone of Shanghai, is now selling *n*-type 100 mm GaN wafers with an epitaxial ready polish.

Eta Research uses the HVPE method to produce GaN wafers. The company says it has completed the R&D necessary for commercialisation of GaN wafers resulting in its HVPE equipment, wafer separation process, and polishing process.

In 2018, the company demonstrated as-grown GaN wafers of 100 mm diameter which can be cut to 2-inch and 3-inch wafers as the finished size. In 2019, the company has developed nearly 5-inch as-grown GaN wafers which can be cut and processed into 100 mm wafers.

The company says it puts a strong emphasis on the importance of the crystal quality and lattice curvature. The typical rocking curve FWHMs of the as-grown wafers are 50 to 60 arcsec for both the (002) and (102) reflections. The threading dislocation density has been measured as 1 x 10^6 cm^{-2} based on CL of polished wafers.

The lattice curvature is important as a measure of the offcut variation across the wafer. The center point offcut is specified at 0.35° toward the GaN *m*-direction and that can be modified according to the customer's requirement. The lattice curvature radius is greater than 10 m, with the target around 30 m or larger.

The company has developed its own polishing process for GaN, resulting in AFM average roughness over 10 µm images of less than 0.3 nm. It has grown MOCVD GaN epi-layers and device structures on the GaN wafers.

Eta Research says that the MOCVD-grown layers show good surface morphology and have XRD rocking curve FWHMs similar to that of the substrate.

Currently, small quantities of 100 mm GaN wafers are for sale, as well as 2-inch and 3-inch wafers. At the end of 2019, more HVPE capacity will be brought online in the new production factory located in Tongling, Anhui Province, China. ET Research anticipates the ability to supply high volume customers in the near future.

Furthermore, working with their epitaxial growth partners, Eta Research can offer GaN wafers with MOCVD epitaxial layers for interested customers.

DuPont sells semi business to SK Siltron

DUPONT ELECTRONICS and Imaging (E&I) has signed an agreement to sell its Compound Semiconductor Solutions (CSS) business to SK Siltron, a silicon wafer supplier based in South Korea. The transaction is expected to close by the end of 2019, subject to customary regulatory approvals for closing.

"The DuPont CSS business has state-of-the-art technologies for SiC wafer production to serve the power electronics market, but it is not a strategic priority for the E&I business," said Jon Kemp, president, DuPont Electronics & Imaging. "Given its strategic focus, we believe SK Siltron will be a better owner and that the CSS business will thrive under SK Siltron's ownership."

According to SK Siltron, the SiC wafers will provide a solid foundation for a new generation of industrial motor controls and power supplies that use electricity more effectively while operating more efficiently. The company plans to combine its manufacturing capabilities with DuPont's research and development to optimise processes.

Mitsubishi announces first multi-cell GaN HEMT on diamond

MITSUBISHI ELECTRIC has announced that in collaboration with the Research Centre for Ubiquitous MEMS and Micro Engineering, National Institute of Advanced Industrial Science and Technology (AIST), it has developed a GaN-HEMT in a multi-cell structure (multiple transistors cells arranged in parallel) bonded directly to a single-crystal diamond heat-dissipating substrate with high thermal conductivity.

The direct bonding of a multi-cell GaN-HEMT to a single-crystal diamond substrate is believed to be a world first. This research achievement was announced at the International Conference on Solid State Devices and Materials (SSDM), held at Nagoya University, Japan from September 2 to 5.

The new GaN-on-diamond HEMT has been designed to improve the power-added efficiency of high-power amplifiers in mobile communication base stations and satellite communications systems, thereby helping to reduce power consumption. Mitsubishi Electric will refine the GaN-on-diamond HEMT prior to its commercial launch targeted for 2025.

Mitsubishi Electric handled the design, manufacture, evaluation and analysis of the GaN-on-diamond HEMT and AIST developed the direct bonding technology. A part of this achievement is based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

Most existing GaN-HEMTs that use a diamond substrate for heat dissipation are created using a GaN epitaxial layer foil from which a silicon substrate has been removed and onto which diamond is deposited at high temperature. HEMTs are then fabricated on the diamond substrate of the flattened GaN wafer. However, because the thermal expansion coefficients of GaN and diamond are different, the wafer can warp greatly during the manufacturing process, making it difficult to fabricate large multi-cell GaN-HEMTs.

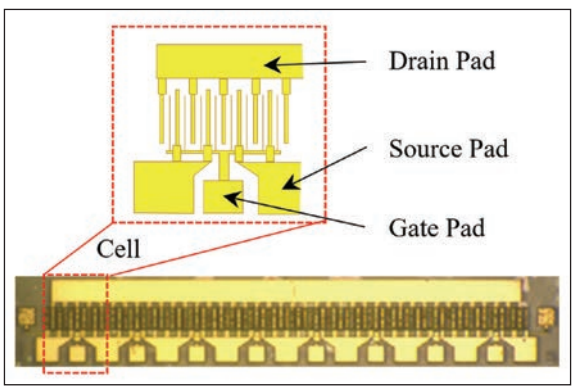
During this research a silicon substrate was removed from a multi-cell GaN-HEMT that was fabricated with a silicon substrate; the back surface of the GaN-HEMT was then polished to make it thinner and flatter, after which it was bonded directly onto a diamond substrate using a nano adhesion layer.

A multi-cell structure was used for the parallel alignment of eight transistor cells of a type found in actual products. Finally, a multi-cell GaN-on-diamond HEMT – the world's first – was fabricated using a substrate with high heat dissipation made of single-crystal diamond.

Using a single-crystal diamond (thermal conductivity of 1,900 W/mK) for superior heat dissipation suppresses temperature degradation, decreasing the temperature rise of the GaN-HEMT from 211 °C to 36 °C.

This improves output per gate width from 2.8 W/mm to 3.1 W/mm as well as raising power efficiency from 55.6 percent to 65.2 percent, thereby realizing significant energy conservation.

There are two completed patents for the technology and nine pending patents in Japan and ten patents pending outside of Japan.



Technology will improve the power-added efficiency of high-power amplifiers in wireless communication

EPC partners with Solace Power

EPC has announced a collaboration with Solace Power, a wireless power, sense and data company, to enable 250 W wireless power solutions designed for 5G, aerospace, automotive, medical, and industrial applications.

Solace Power's intelligent wireless platform uses EPC's 200 V enhancement-mode eGaN power transistors. This modular platform shares the same Equus architecture and enables up to 250 W of transmitted power with superior six degrees of spatial freedom.

"We're excited to collaborate with EPC to further push the limits of our capacitive wireless power platform and to deliver previously unachievable solutions with a higher power requirement," said Solace Power CEO, Michael Gotlieb.

"Solace focuses on delivering complete, modular systems which are pre-tested for CISPR/FCC compliance and optimised in-house for rapid development in real world applications. These new solutions solve the most important challenges for applications requiring 200 watts or more."

For wireless power applications with higher power demands than traditional consumer devices, existing silicon-based transistors become inefficient. To address this limitation, Solace selected a 200 V GaN-based power transistor from EPC for the 250 W solution.

"Wireless power is ready to be incorporated into our daily lives and the modular platform that Solace Power has developed, using highly efficient, low-cost GaN transistors, will improve design cycle times and help new industries implement wireless power quickly and inexpensively," commented Alex Lidow, CEO and co-founder of EPC.

POET Technologies signs deal for sale of DenseLight

POET Technologies has announced that it has signed a definitive agreement with respect to its previously announced sale of its wholly-owned Singapore-based subsidiary, DenseLight Semiconductors. The sale still requires approval from the company's shareholders.

The buyer is DenseLight Semiconductor Technology (Shanghai), a special purpose company recently organised by China Prosper Group on behalf of investors.

DL Shanghai was established to acquire the capital stock of DenseLight from POET for $28 million, which includes $2 million that will be paid to Oak Capital Investment Company, an affiliate of China Prosper Group, for due diligence, negotiation and other services rendered to the buyer in connection with the share sale agreement.

The lead shareholders in DL Shanghai are expected to be Dynax Semiconductors (Suzhou Nengxun High Energy Semiconductor Co.), one of Dynax's major shareholders, the Suzhou Xiang Cheng District Investment Fund and a leading manufacturer of GaAs-based fibre lasers and optical passive devices for high powered lasers. Other shareholders include established funds and investors in the technology and communications industry in China.

Dynax is China's leading developer of GaN-based electronic devices for RF microwave and industrial control in 5G mobile communication and broadband communication. None of the companies or individual shareholders have material interests in businesses that are competitive with DenseLight.

The transaction is expected to close on or before October 31, 2019, with the period between signing and closing allowing for both POET shareholder approval and the activities in which DL Shanghai is currently engaged, including the transfer of ownership interests to investors and assisting with foreign currency transfers prior to the closing.

Following closing, DenseLight's operation in Singapore is expected to be expanded, both to support the preferred supply and strategic cooperation agreements negotiated with POET as part of the Share Sale Agreement and to serve an expanded market presence in China. Future plans include the construction of a high-volume manufacturing plant in Suzhou, expansion of sales and marketing efforts in China and elsewhere, and a potential public listing for DL Shanghai in China.

BluGlass opens new labs in Sydney, Australia

AUSTRALIAN SEMICONDUCTOR technology firm BluGlass formally opened its new Paul Dunnigan Laboratories on Monday 26 August 2019.

The laboratories represent an investment of over $6 million in equipment and associated infrastructure, and incorporate two new cleanrooms at BluGlass' facility in Silverwater, western Sydney. They are named after BluGlass engineer, the late Paul Dunnigan, and will be opened by members of his family, and the City of Parramatta Lord Mayor, Councillor Andrew Wilson.

These laboratories will more than triple BluGlass' capacity and customer output in semiconductor process and equipment development, and will deliver benefits in cost, scale and flexibility to the opto-electronics industry worldwide.

This major facility expansion will help enable BluGlass to export its technology into these high-growth global markets.

BluGlass' Remote Plasma Chemical Vapour Deposition (RPCVD) technology grows semiconductor layers, at atomic levels to very precise tolerances. The process improves on the industry-standard alternative in a number of areas: it operates at cooler temperatures, replaces toxic and expensive ammonia with molecular nitrogen, and provides specialist electronics manufacturers with higher-efficiency devices at lower cost.

The new laboratories will host two new RPCVD platforms. The first of these systems, the BLG-300II, is now commissioned and has started semiconductor wafer growth runs using BluGlass' patented RPCVD process.

BluGlass aims to commission the second, a commercial-scale AIX 2800 G4, towards the end of calendar year 2019, in collaboration with global semiconductor equipment leader Aixtron SE of Germany. It will be Bluglass' largest-ever RPCVD platform.

BluGlass targets a number of specialist global LED markets, including high-performance LEDs, automotive LEDs, microLEDs (use in devices such as smartphones, tablets, and AR and VR systems), and power electronics. Industry researchers estimate that the global LED market will be worth more than $ 96 billion by 2024. (Source: Allied Market Research.)

Giles Bourne, CEO and managing director of BluGlass, said: "BluGlass continues to advance and expand our ground-breaking development to help create the LED technologies and applications of the future."

The new laboratories allow BluGlass to expand its revenue-generating foundry services, continue its RPCVD development and its commercial applications, advance its industry partnerships, and build new production foundations for its continued negotiations with leading specialist electronics manufacturers around the world.

"These developments in western Sydney, first at Macquarie University and now in Silverwater, are proof that Australia can be a world leader in the development of the technologies of the future," explains Bourne.

Andrew Wilson said he was delighted BluGlass has opened its new labs in Silverwater. "These new laboratories are representative of the incredible calibre of research and development that is taking place in the City of Parramatta. I'm pleased to see BluGlass continuing to call Western Sydney home."

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X-Celeprint has used RPCVD *p*-GaN layers to develop an active matrix microLED display prototype. [BluGlass]

Cascade LEDs and beyond

Working with Bridgelux, BluGlass intends to swiftly bring cascade LEDs to market. But this is just the beginning, reports Rebecca Pool

IN A MOVE that marks the latest in a long line of developments this year, BluGlass has signed a joint development agreement with LED manufacturer, Bridgelux, US, to develop cascade LEDs.

The Australia-based developer of remote plasma, chemical vapour deposition (RPCVD) will grow buried activated *p*-GaN layers on wafers, creating tunnel junctions that can be stacked to form cascade LEDs.

Bridgelux will work with BluGlass – as part of the none-exclusive agreement – to evaluate the low temperature, ammonia-free deposition process and tunnel junctions for cascade LEDs. And if all goes to plan, these LEDs will soon be ready for general lighting markets.

"We're taking wafers and growing materials on them using RPCVD, and Bridgelux is going to create and characterise devices, feeding back data to us," says BluGlass managing director, Giles Bourne.

"Our tunnel-junction technology has come on in leaps and bounds in the last year and we can now move reasonably quickly on this."

Industry-wide, cascade LEDs are regarded as a means to mitigate so-called efficiency droop by combining LEDs in a single, vertical stack and generating greater light output for less power. However, conventional MOCVD has, so far, failed to deliver the necessary tunnel junctions at commercial-scale as high-temperature growth introduces impurities to epitaxial layers.

To achieve low-temperature growth, BluGlass has been retrofitting the most common MOCVD systems in the market. The company replaces the ammonia source of an existing system with nitrogen gas, passed through an electrical coil to generate a plasma.

Directly supplying nitrogen via this plasma allows layer deposition at relatively low temperatures, which is crucial to the manufacture of practical GaN-based tunnel-junction devices and cascade LEDs. Earlier this year, the company patented its method to simply and swiftly fabricate the buried activated *p*-(Al, In) GaN layers so critical for tunnel junction function. As Bourne says: "Our process has unique properties so we can grow a very good tunnel junction."

And working with Bridgelux, the managing director reckons devices could reach market within two-to-three years, and possibly a lot sooner. "Bridgelux has very a good front-end technology in terms of devices, and combining this with our low-temperature RPCVD is a good way of accelerating [cascade LEDs] into the market," he says. "Having a partner with oodles of experience of manufacturing devices will help us to get to this endgame."

But general lighting is only the first application that BluGlass hopes to reach with its LEDs that feature tunnel junctions. As Bourne point out, the company has also been developing the technology for UV-LEDs, laser diodes and microLEDs.

BluGlass is currently working with a Europe-based group on microLEDs. And in May this year, Ireland-based BluGlass foundry customer, X-Celeprint, unveiled an active matrix microLED display that uses RPCVD *p*-GaN layers. The prototype has delivered good luminance with colour uniformity, quantum efficiency and forward voltage that equals current high-performance commercial applications of high brightness, 2000 cd/m^2 displays.

Growing plans

To keep pace with the technology growth, BluGlass tripled capacity when it opened new manufacturing facilities – *The Paul Dunnigan Labs* – at its Silverwater site, in August this year. Total investment exceeded $6 million, including the installation of two new reactors that brought the company's deposition system count to five.

A new BLG-300II RPCVD system, based on Aixtron's Thomas Swan 19 by 2 inch reactor, is already online. Meanwhile, a commercial-scale Aixtron 2800 G4 retrofit will be up and running by the end of this year.

"As well as sapphire we have been doing a lot of work on silicon wafers and have a collaboration with a partner that exclusively uses silicon," says Bourne. "We are wafer-agnostic and while the LED industry has been predominantly using sapphire, larger area silicon works well with our low-temperature systems."

BluGlass and Bridgelux are relying on RPCVD to get cascade LEDs to market quickly.

Right now, the company largely deposits layers on 2-inch wafers, but Bourne says scaling to 4-inch and 6-inch wafer sizes is not an issue. And while 8-inch and 12-inch wafers are more challenging, he highlights how systems are configured to handle these larger diameters.

BluGlass also hopes to continue collaborating with Aixtron. As Bourne says: "At the moment our [Aixtron] joint development agreement is really to support the architecture of the tools, but in the longer-term we would like to see how [our technology] can fit into new tool-sets."

"As a business we do not want to get into tool manufacturing... so Aixtron is looking at the technology and how it can be of commercial interest to the company later on," he adds.

And looking to the future, Bourne is excited. "We've got a good baseline technology and I'm looking forward to turning all the hard work from the last decade into commercial output," he says. "Ultimately this is about being part of someone's supply chain – that's what I am really excited about."

X-Celeprint has used RPCVD *p*-GaN layers to develop an active matrix microLED display prototype.

Faster FETs coming soon

Transphorm is set to commercialise GaN epiwafers with a difference, reports Rebecca Pool

AS TRANSPHORM adds more and more GaN FETs to production lines, it recently revealed it is set to manufacture a new kind of transistor technology.

In a $15.9 million project with the US Office of Naval Research, the Californian GaN device manufacturer will fabricate nitrogen polar GaN epiwafers, with a view to providing the first commercial source of material for domestic RF and power electronics markets. As Transphorm co-founder and chief operating officer, Primit Parikh, tells *Compound Semiconductor*: "Now the science has been proven, the Department of Defense wants a commercial source of this material."

"Many of its clients are working on GaN devices, so a manufacturing-scale supply of the nitrogen-polar GaN epitaxial materials is going to be important," he adds. "We already have multiple MOCVD reactors but through this programme we will be able to add to our existing capability."

While high-voltage Ga-polar GaN devices are making in-roads into myriad RF and power electronics applications, N-polar versions have lagged in development. When growing GaN on a foreign substrate, the material naturally nucleates to form Ga-polar GaN. What's more, the N-face of GaN is less thermally stable than the Ga-face, making subsequent N-polar material growth on N-polar GaN more difficult.

However, researchers from the US-based University of California, Santa Barbara, led by Umesh Mishra, and also sponsored by the US Office of Naval Research (ONR) and the Defense Advanced Research Projects Agency (DARPA), have spent more than a decade honing this technology. And crucially, they have now demonstrated millimetre-wave devices with, as they claim, record power densities and high efficiencies.

"[We have reversed] the N-polar orientation of the material from the traditional Ga-polar GaN, currently used in base station and Department-of-Defense applications," highlights Mishra. "This flip produces radical benefits in output power along with ground-breaking efficiencies to frequencies as high as 94 GHz."

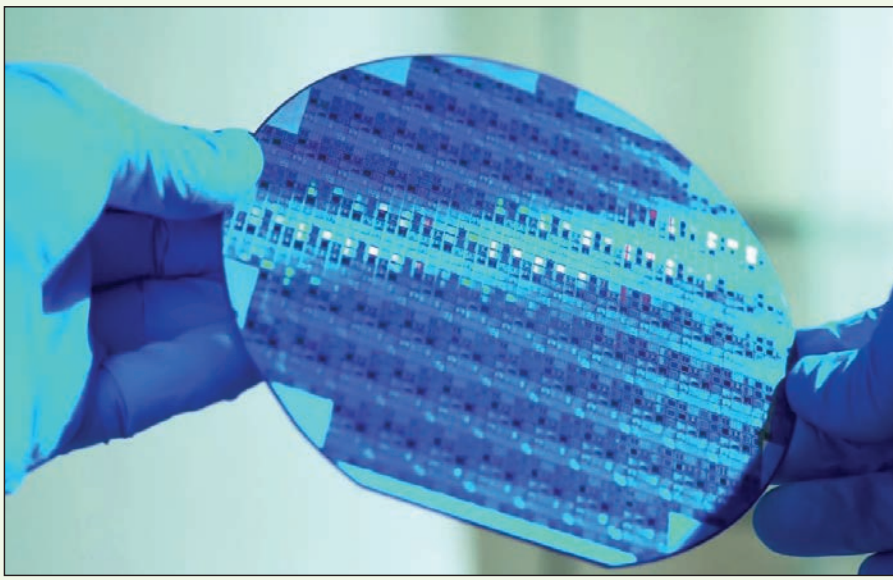
"Applications span the frequency range of interest for 5G and 6G, and beyond, and also fill a critical technological void for DoD systems," he adds.

Details on the polarisation engineering behind the development of N-polar structures and devices are scant, but Parikh is confident that he and his colleagues can now make the material manufacturable on a commercial-scale.

"A lot of research has gone into producing a good quality material that can be manufactured on large-area wafers, and this is the crux of what Transphorm is now doing with this contract," he says.

According to the CTO, Transphorm will grow N-polar GaN layers on SiC and sapphire substrates for RF applications, but switch to silicon for power electronics applications. "We are working with GaN-on-silicon as power electronics devices [follow] a different kind of performance-cost roadmap ," he says. "And because of the SiC shortages we also want to work on developing this with sapphire substrates as well [for RF applications]."

Substrate sizes will include 4-inch and 6-inch wafers, and ultimately 8-inch wafers, although work on the largest wafer size will be, as Parikh says, dictated by market demand.



"In the future, [development on eight-inch substrates] will be market driven and this is going to take several years," he says. "At Transphorm, when we say we are ready, we mean we are ready for manufacturing and not just demonstrations, so work has to be done, but this is a natural progression and all the proof-points exist."

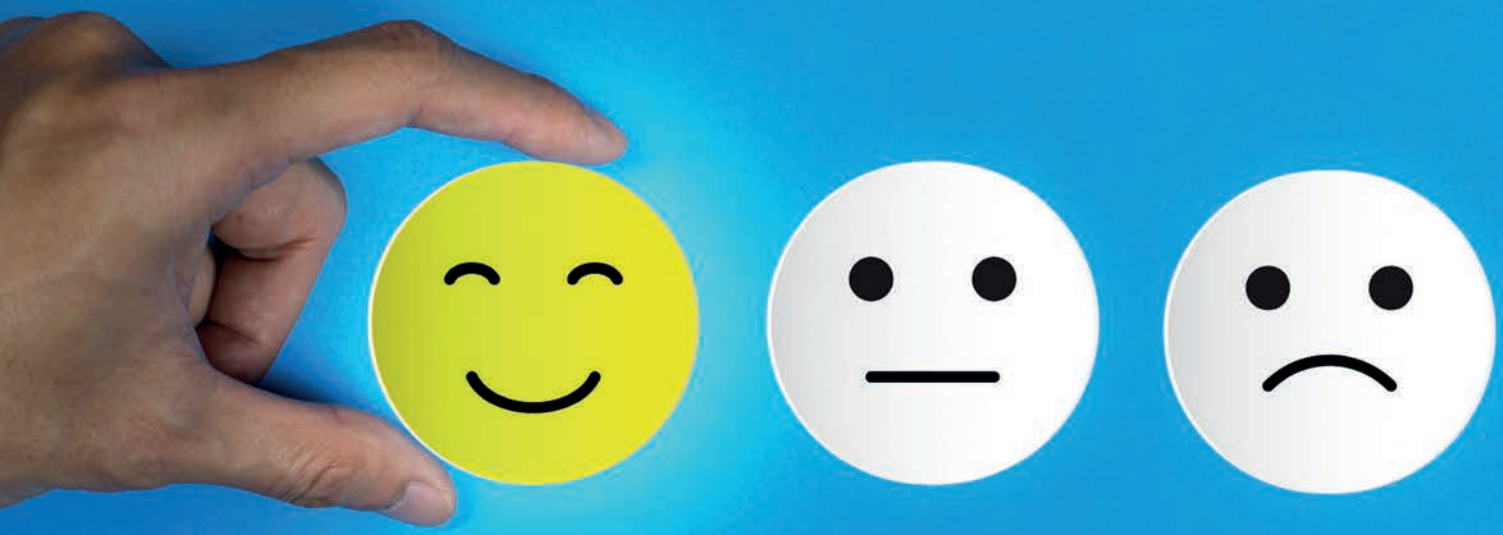
So what now? According to Parikh, technology and manufacturing will be prioritised in the project's first year, with production scaling following. "We will be scaling up our uniformity and yield, and demonstrating this, especially on the RF side," he says.

Come the end of the project, 2022, technology and manufacturing maturity will have transitioned from the DoD's early-stage Technology Readiness Levels (TRL) and Manufacturing Readiness Levels (MRL) to the latter, proven levels of MRL8, 9 and TRL8, 9. And after this time, the mature devices will undergo qualification.

"We expect that after the project, the devices made by our customers will get traction and continue to mature as more and more devices are qualified and released," says Parikh. "The government's long-term vision is to see these devices making their way into systems."

And crucially for Transphorm, the project allows the company to not only expand MOCVD production of GaN-based devices but also develop vertical epiwafer sales for DoD customers as well as RF and 5G markets.

"We are already seeing demand and are excited to go from purchase to production in less than 36 months, a key programme goal," says Parikh.



Evaluating the substrate market

RICHARD STEVENSON QUIZZES YOLE DÉVELOPPEMENT'S HONG LIN AND EZGI DOGMUS on the state-of play on all the major compound semiconductor substrate markets, and what the future might hold for them.

Q The Wolfspeed division of Cree has been making the headlines for exclusive wafer supply agreements. In the last year or so, it has signed a deal with Infineon that is worth over $100 million, one with STMicroelectronics valued at $250 million, and it has entered into two additional contracts, each worth over $85 million – one with ON Semiconductor, and the other is with an undisclosed power device manufacturer. What does this tell us about SiC substrate supply in this industry?

HL: The wafer is the key to the power SiC industry. There has been a shortage of supply in the market since 2016. Wolfspeed have invested significantly to produce their wafers. They have a dominant position, and they are quite likely to keep that position for at least the next two or three years, without any problems. They have some competitors, such as II-VI, and newcomers, such as GTAT and other players – but those players are not likely to take Wolfspeed out of the number one position.

Q Is the quality of 6-inch SiC still lagging that of 4-inch SiC?

HL: We cannot generally say that it is lagging. It is player dependent. There are players that are able to

produce very good 6-inch quality. I think we are in a transition to 6-inch, and 6-inch will be really dominant in the coming years.

The wafer quality is slightly different for diodes and MOSFETs. MOSFETs have more stringent requirements. When you are talking to suppliers, there are different qualities of wafers. There is premium quality and medium quality, and the lead times are different, pricing is different.

What is the SiC substrate market worth today, and how fast will it grow in the coming years?

HL: If we are talking about the power electronics market, today the market size is more than $100 million. But SiC is not just used for power electronics. It is also used for GaN-on-SiC for 5G applications. Together, the market size is more than $150 million. In both these markets we see double-digit growth.

With the rise of internet streaming, sales of BluRay players have fallen. Has this impacted sales of GaN substrates, which have provided the foundation for making lasers for BluRay players?

HL: Bulk GaN was initially used in lasers for BluRay players. The fall in BluRay sales has not been good news for makers of bulk GaN substrates. But GaN is still used for laser diodes in other applications. They are taking off, so there is a kind of balance.

At some point in time there was some hype about GaN-on-GaN LEDs. This technology was pursued by the US company Soraa. But I think that excitement has past.

There is interest in GaN substrates for making vertical GaN-on-GaN power devices. Has this translated into sales yet?

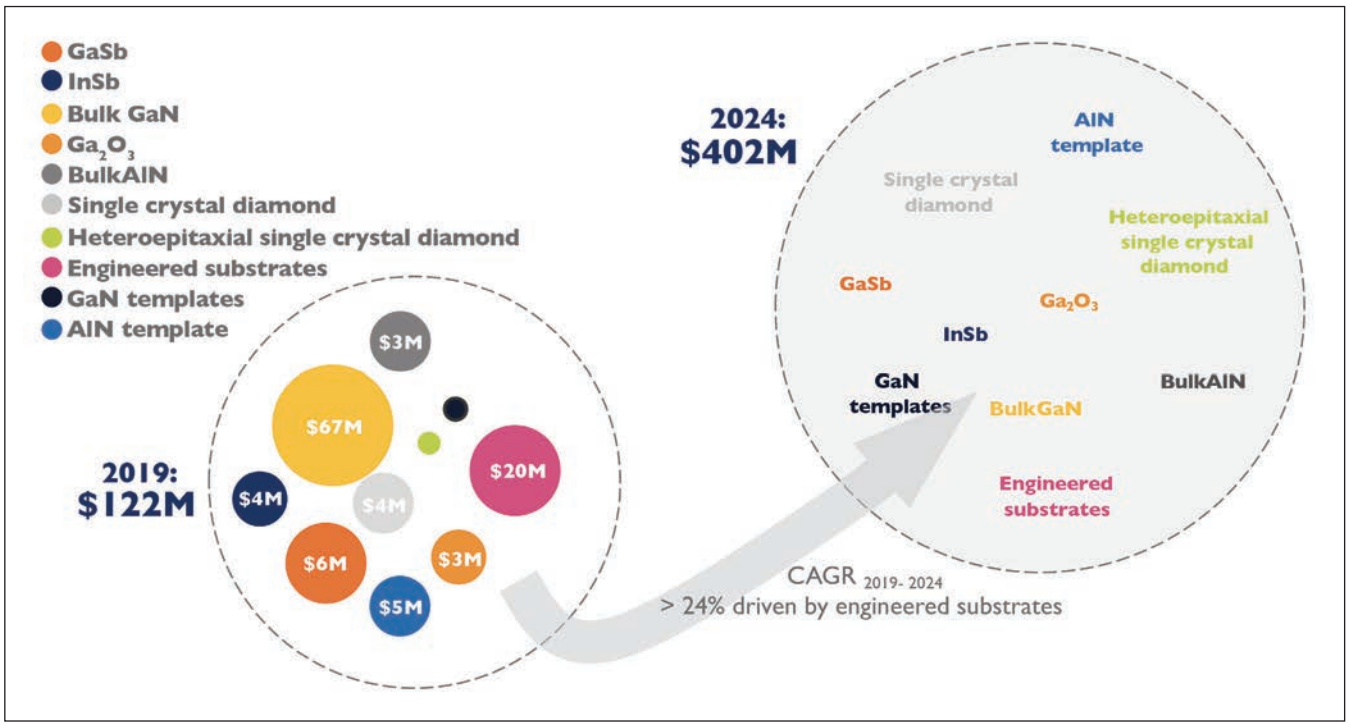
HL: I don't see any real commercial product. There is a lot of research, an increasing number of patents, and an increase in discussions about this at conferences. But we are still in the early phase of GaN-on-GaN power technology. If we compare to SiC, GaN-on-GaN is at least ten years behind.

Does Sumitomo still dominate the market?

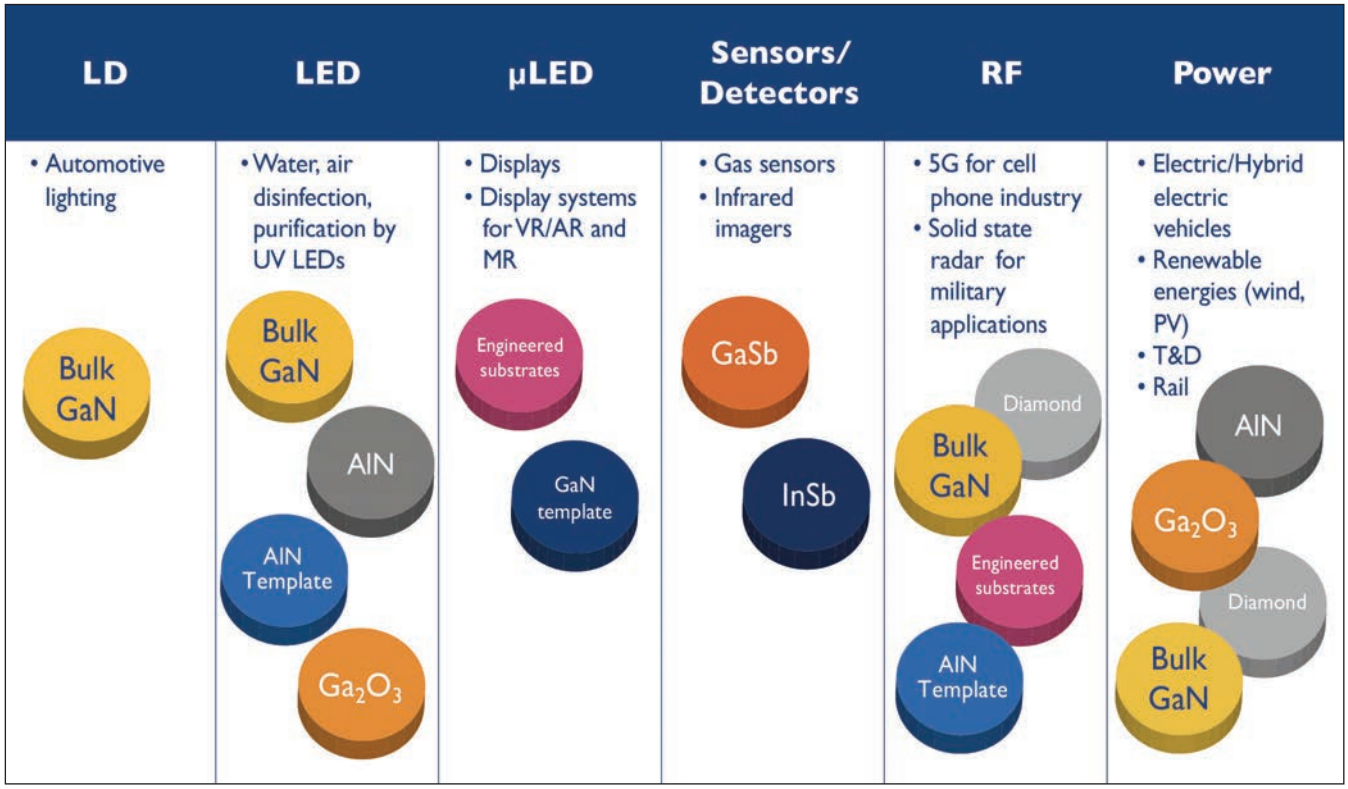
HL: The market is dominated by Japanese players. Not only Sumitomo Industries, but also SCIOCS and Mitsubishi Chemical.

Do you think that the ammonothermal growth method for GaN will make a commercial impact? The Polish-firm Ammono failed to enjoy significant success but the Californian company Six Point Materials has high hopes?

HL: Ammono went into bankruptcy, but they have been taken up by the Polish Institute of High Pressure Physics. So it's not 100 percent closed – there is still some pilot-line capability. Six Point have started to make 2-inch material. Development will take time.



The total market revenue for emerging materials will more than triple between 2019 and 2024.



Over the next five years, markets will grow that offer new opportunities to a range of compound semiconductor substrates.

There is much interest in ultra-wide bandgap materials, including AlN and gallium oxide. I understand that AlN is incredibly difficult to produce. Are there any significant commercial suppliers?

HL: For AlN, there is commercial product. There are 2-inch wafers available from Hexatech in the US. There are start-ups acquired by Japanese companies, and they have commercial products. There are 2-inch commercially available materials, but AlN remains a small market as of 2019 in our understanding.

For gallium oxide, crystals can be produced using established growth methods. How mature is this market, and who are the biggest players?

HL: For gallium oxide, we have ten to fifteen years of delay compared with SiC in power electronics applications. Of course, gallium oxide has a lot of application possibilities.

I think the biggest player is Tamura. Novel Crystal Technology is there spin off. The closest to commercialisation at the device level is the Japanese start-up Flosfia. And you have development in the US, particularly for military applications.

Gallium oxide is still very far from commercialisation. But like vertical GaN, if you look at the number of publications per year, or the number of patents, they are increasing. I would not be surprised if in two or three years we will see a lot of start-up companies providing wafers. At the beginning of a new material, there will be a lot of small companies. If we look at the device level, diodes or MOSFETs, the progress is very significant over the last five years.

What is the primary use for GaAs substrates? Is it to make the power amplifiers for mobile phones?

ED: One of the main applications for GaAs is the power amplifiers in mobile phones. We hope to see GaAs in 5G phones, so it will still have its position in the RF industry.

Is there much demand for GaAs substrates for LEDs, lasers and solar cells?

ED: We see for the LEDs, the GaAs market is quite big. With GaAs, the bandgap is quite suitable for red and infrared applications. In the large display technologies, you see GaAs being used for red LEDs. This is a domain that is emerging, because you need more resolution, so you need smaller LEDs, and more and more LEDs in a display. So it will increase, a lot, the GaAs LED market.

We also see the laser market going up for GaAs. You will have heard of Apple using the GaAs VCSELs – the vertical-cavity, surface-emitting laser. They are used for 3D sensing, for facial recognition. This has produced a big change in market dynamics. Instead of more GaAs [edge-emitting] lasers, we see more Android users adopting this solution.

For the solar cells, the market is still small. A long time ago there was hope for GaAs for high-efficiency solar cells. But in the beginning of 2010s, we saw silicon solar cells decrease a lot in price, and the competition has become very tough. That's the smallest market for GaAs substrates today.

I understand that there has been a substantial fall in the average selling price of GaAs substrates over the last few years. Is that correct?

ED: The average selling price is application dependent. For RF, which is a big, stable market, we do not see a big decrease in the ASP. It is a similar situation for the LED. But for the VCSEL, there will be some price erosion over the next few years, because there is a big interest in this domain, due to 3D sensing and other VCSEL applications.

Who are the leading suppliers of GaAs substrates?

ED: There are three big suppliers of GaAs substrates: the German company Freiberger; Sumitomo of Japan; and the US company AXT, which is also based in China.

What are the most popular diameters for GaAs substrates?

ED: It is application dependent. For RF, for power amplifiers in handsets, it is 6-inch. For LEDs, we see more 4-inch. With VCSELs, we see a transition to 6-inch, and we think it will stay at 6-inch.

HL: For GaAs, the wafer quality is application dependent. Chinese players are developing material for the low-end, for LED applications. The market share, in dollars, is small, but the volume could be quite high.

For InP substrates, are telecom lasers the biggest application?

ED: For lasers, the biggest applications are telecom and datacom. Increases in volume are driven by datacom applications, with Google, Amazon and other players implementing data centres. For telecom applications, this market is also increasing. As volumes are increasing, we are expecting the price to fall.

Which companies are dominating the InP substrate market?

ED: There is AXT, Sumitomo and JX Nippon. They are the top three players.

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InP DHBTs
eye millimetre-wave 5G

Optimised InP DBHTs deliver the high breakdown and the low knee-voltage required for high-efficiency 5G power amplifiers

BY YUEFEI YANG, DHEERAJ MOHATA, DAVE RASBOT, RICARDO SOLIGO AND DAVID WANG FROM GLOBAL COMMUNICATION SEMICONDUCTORS AND ROBERT BAYRUNS, JOHN BAYRUNS, DAVID OSIKA AND JOSEPH BRAND FROM DUET MICRO ELECTRONICS

THE 5G NETWORK will roll-out in two phases. The first of them, involving frequency bands below 6 GHz, is already being deployed in several cities in different countries. Following in several years will be the second phase, offering higher data rates, greater capacity, better quality and lower latency.

Deployment of the second phase involves the introduction of frequencies within the millimetre-wave K_a-band that spans 24 GHz to 40 GHz. These higher frequencies will enable the delivery of multi-gigabit speeds to homes, apartments and businesses, in the form of millimetre-wave fixed wireless access, featuring phase-array beam-steerable active antennas and massive MIMO (multiple inputs, multiple outputs).

Throughout the evolution of wireless technologies, the power amplifier (PA) has been a critical component

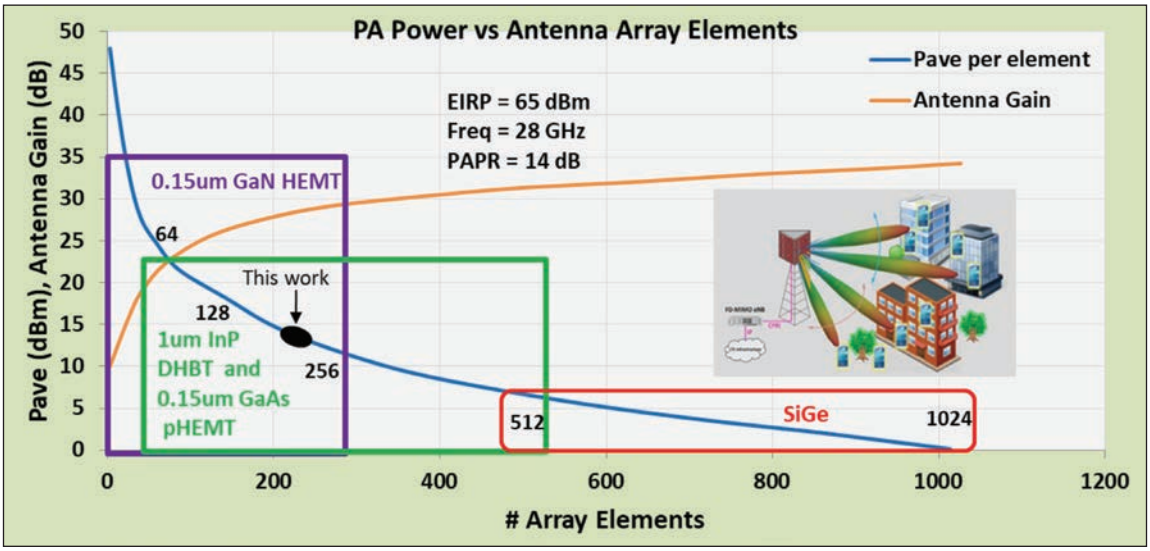


Figure 1. The required PA power and antenna gain for a varying number of antenna elements. GaN HEMT and InP DHBT PAs need fewer antenna elements, due to their high power capability; while SiGe BiCMOS need more elements, due to their low power capability.

within the active antenna of every connected device. In today's 3G-4G LTE market, the dominating technologies for this form of amplifier are the GaAs HBT and silicon LDMOS. The former offers performance, as well as flexibility of manufacturing, while the latter majors on maturity, low cost and a high level of integration.

At millimetre-wave frequencies, neither of these technologies is expected to fulfil the performance requirements, due to inherent material limitations. More promising are the 0.15 μm GaN HEMT, the 0.15 μm GaAs pHEMT, the micrometre InP DHBT, and nanoscale silicon CMOS and SiGe BiCMOS technologies.

Power amplifier considerations

Efforts are underway to determine the best design for the active antenna array elements in 5G millimetre-wave fixed wireless access systems. For the antenna, the effective isotropic radiated power (EIRP) is typically 65 dBm. This target can be met in many ways – it can be fulfilled with a small number of high-power PAs, such as those formed with GaN HEMTs; or it can be met with far more lower-power PAs, like those made from silicon CMOS or SiGe BiCMOS (see Figure 1 for an overview of various options). Note that selecting a large number of antenna elements with silicon CMOS or SiGe BiCMOS could result in a more expensive, less efficient solution.

A useful rule of thumb is that if a given technology is to be useful at a given frequency, its maximum oscillation frequency for power gain, a metric known as f_{max}, must be at least four times its operational frequency. So, for operation at 28 GHz, f_{max} should be 120 GHz or more.

There are several downsides to using HEMTs for amplification at these frequencies. Whether made from GaN or GaAs, the gate length must be no more than 0.15 μm. In compound semiconductor fabs, such a short gate length tends to be reached with electron-beam lithography, which is often a very high-cost,

PA technology (Ka Band)	Cost and Complexity				Performance				
	Subs Cost	Die Size	Supply Polarity	Litho complexity	BV	V_{KNEE}	PAE	Linearity	Power Density
0.15um GaN/Si HEMT	Low	Large	Bipolar (Dmode)	High	High	High	Poor	Poor	High
0.15um GaAs pHEMT	Low	Large	Unipolar	High	Med	Low	Avg	Poor	Med
45nm CMOS/ BiCMOS	Low	Large	Unipolar	Low	Low	High	Poor	Poor	Low
InP DHBT	Med	Small	Unipolar	Low	High	Low	High	High	High

Table I: Manufacturing cost, complexity and performance comparison between PAs from competing technologies for 5G K_a-band millimetre-wave applications.

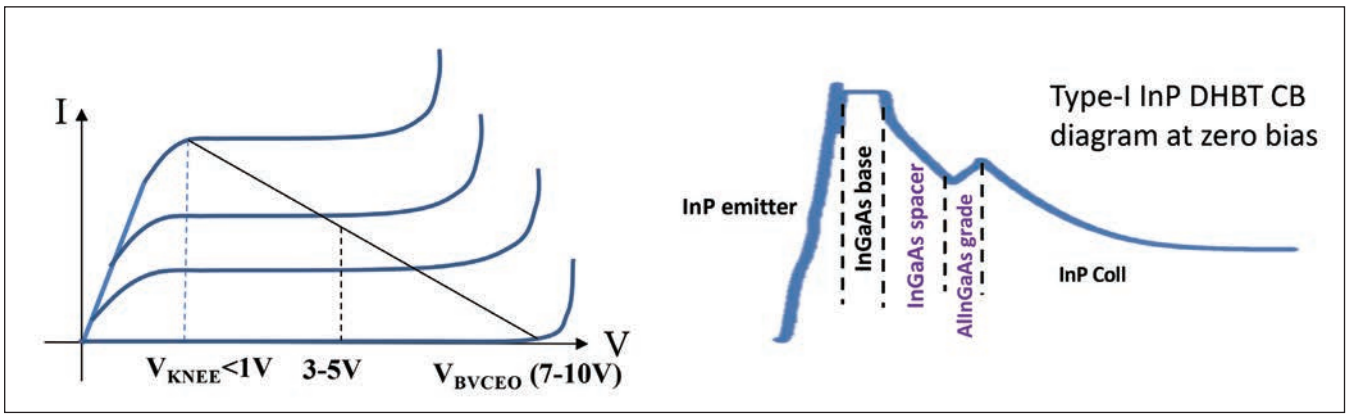


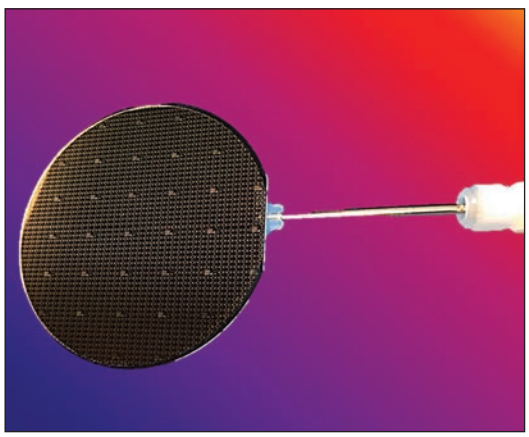
Figure 2. (Left) Output family of current-voltage curves for a power transistor showing the desired knee-voltage (V_{KNEE}) and breakdown voltages to maximise the output power while maintaining good efficiency. (Right) Conduction band diagram showing the presence of a barrier between an $In_{0.53}Ga_{0.47}As$ base and an InP collector. Spacer and grading layers smooth out the band-discontinuity and move it away from the junction.

low-throughput solution. Another issue is related to the operation of the HEMT. To realise a high power, it must be driven with a high supply voltage, and withstand a high breakdown voltage. Realising very high breakdown voltages and delivering very high powers are well within reach of the GaN HEMT, but this transistor – and also the GaAs D-mode pHEMT – requires negative supplies for the gate bias, and the inclusion of a device that acts as a drain cut-off switch. These additions contribute to cost and complexity. And on top of these drawbacks, HEMT technologies intrinsically suffer from poor linearity and a low power-efficiency.

A promising alternative to the HEMT is the InP DHBT. It is renowned for its high speed, high linearity, high power efficiency and low off-state leakage current – a set of attributes that are highly desired for handset applications. Short gate lengths are not an issue, as the minimum feature size can exceed 1 μm, making this device easy to manufacture with high throughput in any III-V fab.

One of the concerns with the InP DHBT is the high cost associated with both the substrate and the epitaxial process. Although InP substrates are needed for making lasers, the devices are very small, so substrate volumes are not substantial. But they could be, leading to lower prices, if production of the InP DHBT takes off.

Another challenge is that when the InP DHBT targets millimetre-wave PA applications, it tends to be compromised by the low collector-to-emitter breakdown voltage, BV_{CEO}. This stems from the use of un-optimised narrow bandgap InGaAs in the base-collector junction.



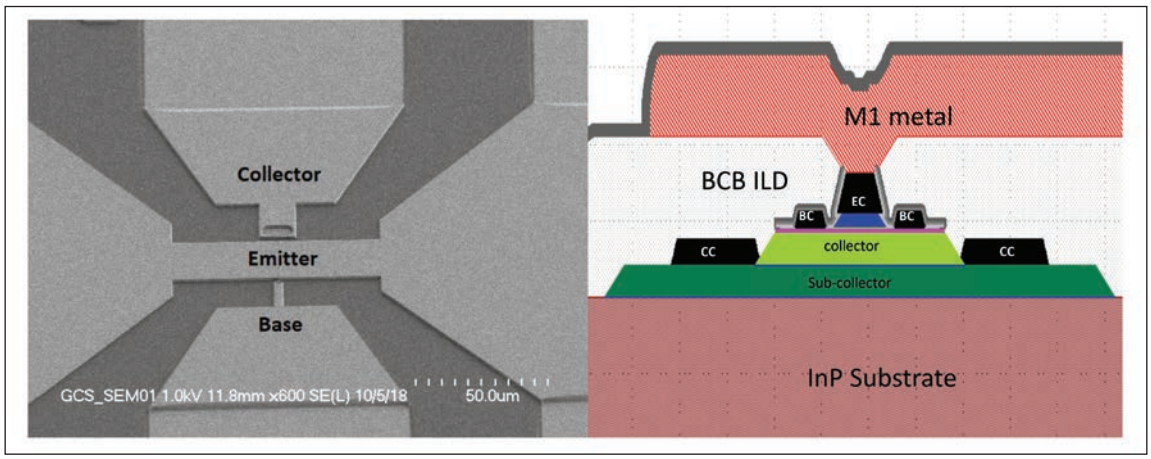


Figure 3. (Top) Processed 4-inch InP DHBT wafer, held using a vacuum wand. (Bottom left) Tilted view scanning electron micrograph showing metal 1 routing to the base, collector and emitter contacts of the DHBT. (Bottom right) Cross-section of a typical GCS InP DHBT.

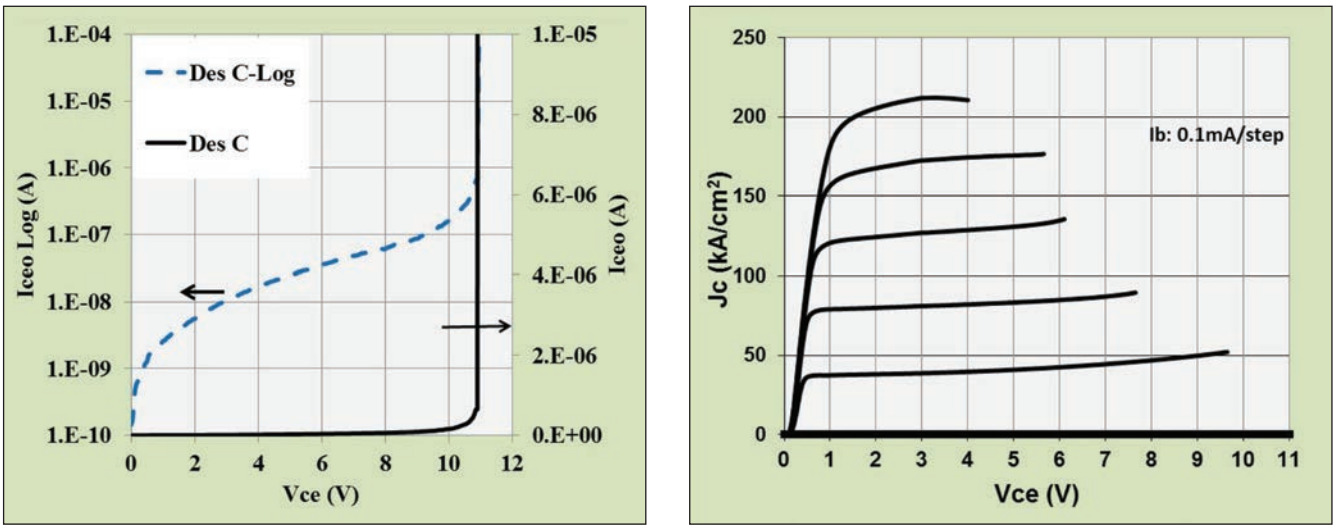


Figure 4. (Left) I_{ceo} verses Vce for optimised InP/$In_{0.53}Ga_{0.47}As$ DHBT epi design. Device size is 1.6 μm by 10 μm. The collector-emitter junction achieves sharp breakdown and low leakage. (Right) Output current-voltage curves show low knee-voltage characteristics.

At Global Communication Semiconductors LLC, working in partnership with a team from Duet Micro Electronics, we have addressed the low breakdown voltage in these devices. Our success comes from optimising the transition layers in the base-collector junction by fine-tuning the doping and the thickness. This has enabled the production of InP DHBTs with a level of performance that makes them an attractive candidate for 5G networks.

Increasing the breakdown voltage

During the typical operation of a power amplifier, the output voltage swing peaks at twice the operating voltage. So, in cellular applications where the operating voltage is often between 3 V and 5 V, output voltage swings can hit 10 V. Ideally, this requirement is met while ensuring that the knee-voltage is below 1 V at a collector current density of more than 100 kA cm^{-2}, as this allows the output power to be maximised while drawing on the full benefits of envelope tracking (see Figure 2, left).

The key to meeting all these requirements is to optimise the base-collector junction. The type I band alignment between the $In_{0.53}Ga_{0.47}As$ and InP layers creates a significant energy barrier for electrons transiting from the base to the collector (see Figure 2 right). Normally, in this region of the device there is an $In_{0.53}Ga_{0.47}As$ spacer and a quaternary grading layer made of an InAlGaAs alloy, a combination that smooths out this discontinuity or moves it away from the base-collector junction. The trick is to choose the right combination of thicknesses and doping, to ensure good trade-offs between: the unity gain cut-off frequency, f_T; the maximum oscillation frequency, f_{max}; the breakdown voltage, BV_{CEO}; and the knee voltage, V_{KNEE}.

By improving the design of the epilayers in our InP/$In_{0.53}Ga_{0.47}As$ DHBT, we have increased the BV_{CEO} of our transistors to around 11 V. Devices with this level of ruggedness have been made by processing 4-inch InP epiwafers, produced by solid-source MBE (see Figure 3 for an image of the processed wafer, along with a tilted-view scanning electron microscopy image of the fabricated DHBT, and a cross-sectional diagram of the DHBT, including the contact layers).

We have measured the collector-emitter leakage curves of our transistors, along with their output current-voltage characteristics (see Figure 4). Collector-emitter breakdown behaviour is abrupt, implying that the material has reached its intrinsic breakdown. The knee voltage is low, measuring just 0.6 V at a collector current density of 120 kA cm^{-2}.

The high-frequency performance of our transistors is very encouraging. We have measured an f_T of 115 GHz and an f_{max} of 150 GHz (see Figure 5).

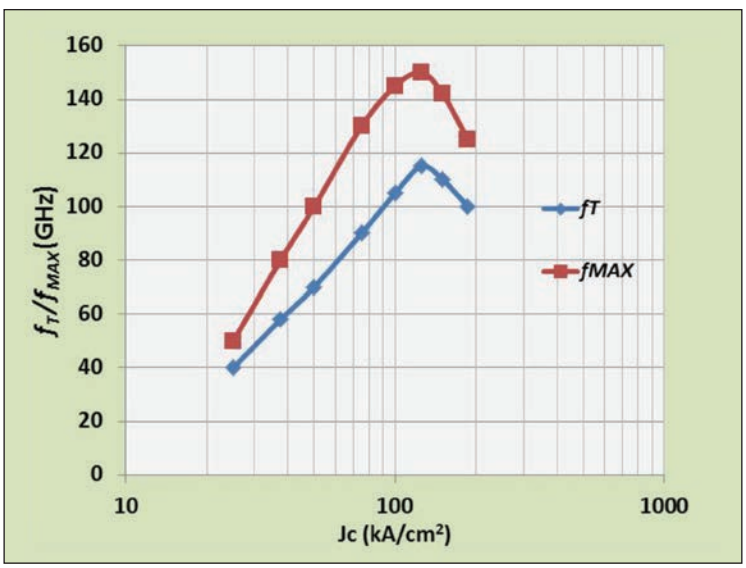


Figure 5. f_T and f_{max} versus the collector current density, Jc, for a DHBT with emitter size of 1.6 μm by 10 μm. Maximum f_T of 115 GHz and maximum f_{max} of 150 GHz are obtained.

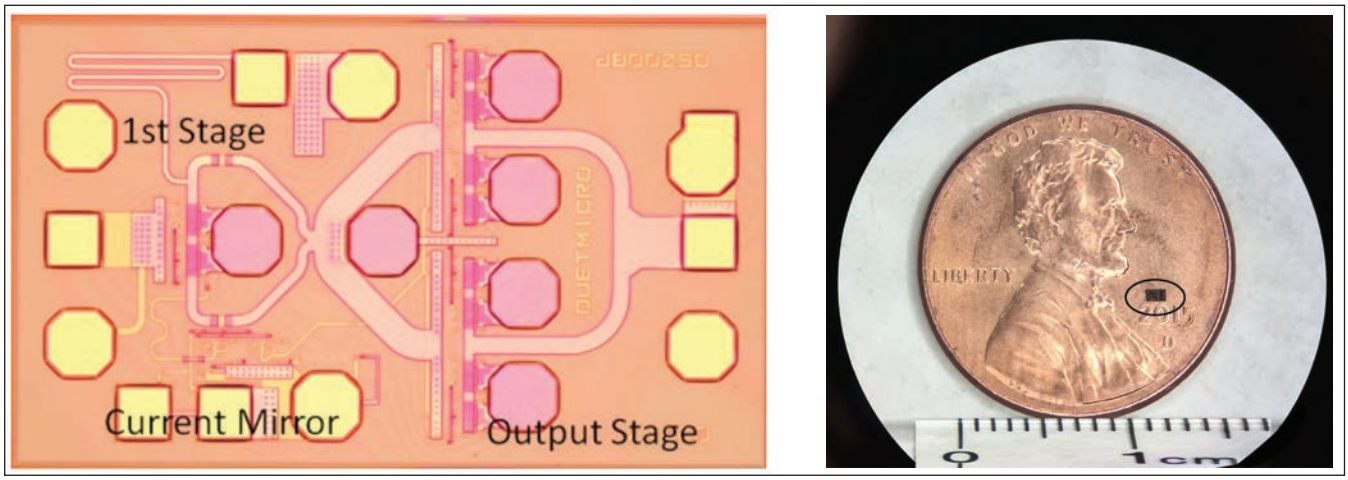


Figure 6. (Left) Optical micrograph of a two-stage power amplifier using InP DHBTs. (Right) Comparing die size to that of a nickel dime. Die size is 0.7 mm by 1.2 mm. In this amplifier, the first stage input has a bandpass match topology; the inter-stage match is low-pass as well as the final output match.

These values, plus those for the breakdown voltage and the knee-voltage, indicate that our InP DHBT is a very good device for K_a-band operation.

A two-stage amplifier

Drawing on our optimised DHBT, we have designed and fabricated a two-stage power amplifier (see Figure 6 for images). Die size is just 0.7 mm by 1.2 mm, making our amplifier far smaller than other technologies – a valuable trait given the premium placed on a small footprint inside the smartphone. Within the circuit there is a CMOS compatible-current mirror, which supplies a reference current to the first and second stages. To minimise the effects of through-wafer via inductance, the output stage is divided into four power-cells, combined at the inputs and outputs.

Measurements on this amplifier, run at an operating voltage of 3 V, show a gain of about 18 dB between 27.5 GHz and 28.35 GHz (see Figure 7, left). At this operating voltage, a power sweep at 28 GHz reveals a saturated power, P_{SAT} of about +26 dBm when the circuit is driven 5 dB into compression. At this condition, the measured power-added efficiency, PAE, is 54 percent (see Figure 7, right).

These measures of performance allow us to determine the number of elements in an array. The good news is that this figure is 256, far less than the number required for silicon CMOS or SiGe BiCMOS technologies. And simulations suggest that an even lower number is possible. Increase the operating voltage to 5 V, the P_{SAT} is expected to hit 30.4 dBm, allowing the number of elements to fall to a more

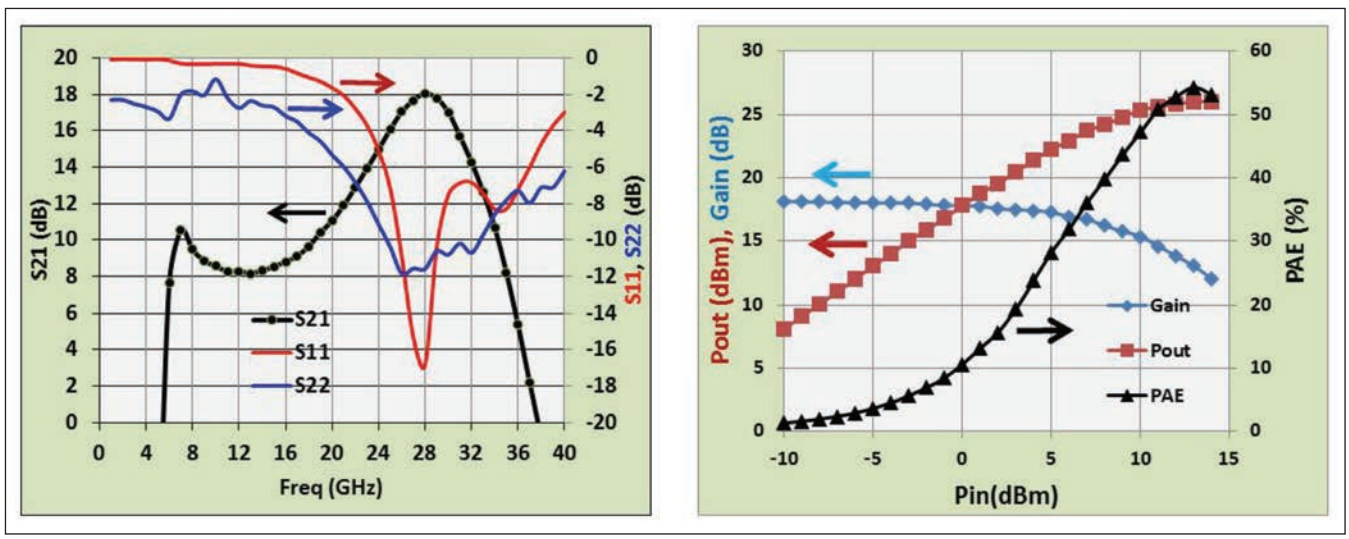


Figure 7. (Left) Measured S-parameters as a function of frequency. S21 is 18 dB at 28 GHz. The input match provides an S11 from -17 dB to -12 dB, while the output S22 is better than -10 dB across the band, indicating good matches for both input and output stages. (Right) Power sweep results showing power-added efficiency of 50 percent and a saturated power output of 26 dBm for a two-stage PA. Backed-off, the P1dB is +24 dBm.

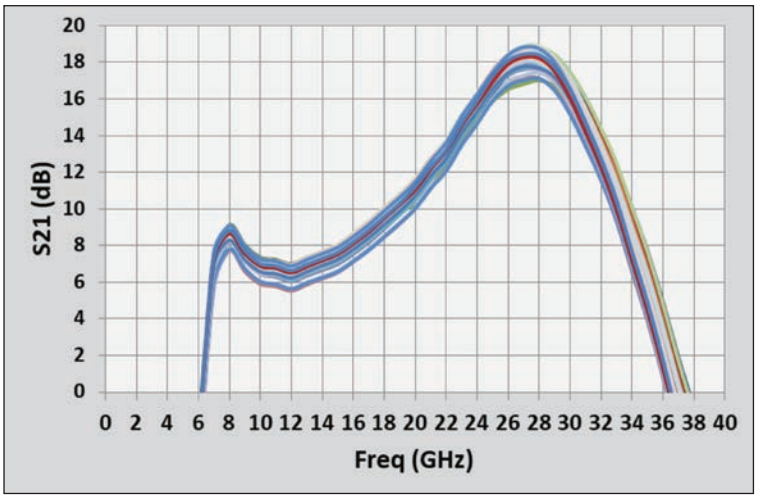


Figure 8. On-wafer S21 curves at multiple sites across a 4-inch wafer showing good uniformity.

usable 128 (see Table 2 for a detailed evaluation of our technology, compared with 45 nm SOI CMOS, 0.13 μm SiGe BiCMOS, 0.15 μm GaAs pHEMT and 0.15 μm GaN HEMT).

Another encouraging sign for our technology relates to the plots of S21, the power transferred from port 1 to port 2. We have measured this figure for about 100 die across a 4-inch wafer. Results highlight good PA performance uniformity across our wafer.

Our work makes a strong case for the InP DHBT millimetre-wave PA in fixed wireless access and handset applications. It's not just that the overall PA performance is better; the process is simpler, and the chip size is smaller than rival technologies. What's more, it offers a single supply voltage, and the low power-down DC leakage current for the InP DHBT PA is especially attractive for handset applications.

So far, we have made PAs that use an emitter with a device size of 1 μm by 10 μm. We plan to progress to a larger optimum device size as we strongly believe that this will deliver further improvements in the performance of the PA, including a hike in the output power. This will get an additional boost by upping the operating voltage to 5 V. To assess the extent of these benefits, we are currently preparing to run a 'design-of-experiments' programme.

Our efforts are also being directed at evaluating InP DHBTs that are grown on lower-cost substrates, such as GaAs or silicon. We want to determine if it is possible to maintain the performance of the PA with substrates that are lower in cost and less brittle.

A third goal for our team is to carry out extensive reliability studies. Demonstrating the reliability of our InP DHBT will allow it to win substantial orders in K_a-band PA applications, and ultimately provide the best solution for millimetre-wave 5G networks.

Further reading

SNS Telecom. "5G for FWA (Fixed Wireless Access): 2017-2030-Opportunities, Challenges, Strategies & Forecasts

D. Schnaufer *et al*. "Delivering 5G mmWave fixed wireless access" EDN, September 2017

Y. Yang *et al*. "Development of InP DHBTs with High Breakdown Voltage for K_a-Band PA Applications", International Conference on Compound Semiconductor Manufacturing Technology, Minneapolis, MN, 2019.

Measured Parameters	Unit	1 μm InP DHBT [This work]	45 nm SOI CMOS	0.13 μm SiGe BiCMOS	0.15 μm GaAs pHEMT	0.15 μm GaN HEMT
V_{CC}/V_{DD}	V	3	2.4	1.5	4	20
I_{CC}@ P_{SAT}	mA	235	NA	NA	NA	NA
PA Off Current	μA	<1	NA	NA	NA	NA
Frequency	GHz	28	28	28	28	29
Gain	dB	18	10	18.2	21.3	22
P1dB	dBm	24	21.5	15.2	NA	NA
P_{SAT}	dBm	26	22.4	23.7	31	39
Peak PAE	%	54	40	20.3	27.3	30
Die Size	mm^2	0.84	0.63	1.76	4.5	11.2

Table II: Summary of the two-stage PA of this work and comparison with other technologies.

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OBLITERATING THE THERMAL BARRIER IN GAN-ON-GAN DEVICES

Thermal analysis reveals that backside processing reduces the rise in the temperature of GaN-on-GaN devices

BY NAOYA OKAMOTO FROM FUJITSU LIMITED AND FUJITSU LABORATORIES

The GaN HEMT is renowned for delivering a high RF output power at a high efficiency. Thanks to these qualities, this class of transistor can dramatically improve the performance of microwave to millimetre-wave radio communications and radar systems. These HEMTs could be used in weather radar systems, monitoring and predicting local heavy rainfall, and in 5G systems, providing communication in the millimetre-wave band.

Yet another opportunity for the GaN HEMT is as a successor to the conventional magnetron, providing heating in microwave ovens. This modification would usher in an era of innovative, compact microwave heating. Turning to HEMTs would suppress wasteful energy consumption by irradiating only the heating region with microwave energy.

The majority of commercially available RF GaN-based HEMTs are fabricated on SiC substrates. Using this foundation, the crystal quality of GaN is higher than it is for growth on sapphire and silicon, while the substrate combines a high thermal conductivity with excellent insulation (see Table 1 for a more detailed comparison of different substrates for GaN).

Efforts are underway all across the world to drive the output power and efficiency of the GaN HEMT to a new high, because this would lead to further improvement in system performance. That's not easy, though, as GaN HEMTs are plagued by current collapse, which significantly diminishes drain efficiency. The primary cause of this malady is electron trapping, taking place at the buffer layer and at the interface between GaN and the passivation film, typically SiN (see Figure 1). A root cause of this issue is the high density of dislocations in the buffer layer, arising from growth on lattice-mismatched substrates.

An effective approach for quashing the dislocation density is to grow the epilayers on freestanding GaN. This substrate, which has a dislocation density of the order of 10^6 cm^{-2} or less, enables a reduction in the dislocation density of the GaN epitaxial layer by at least two orders of magnitude compared with the SiC substrate.

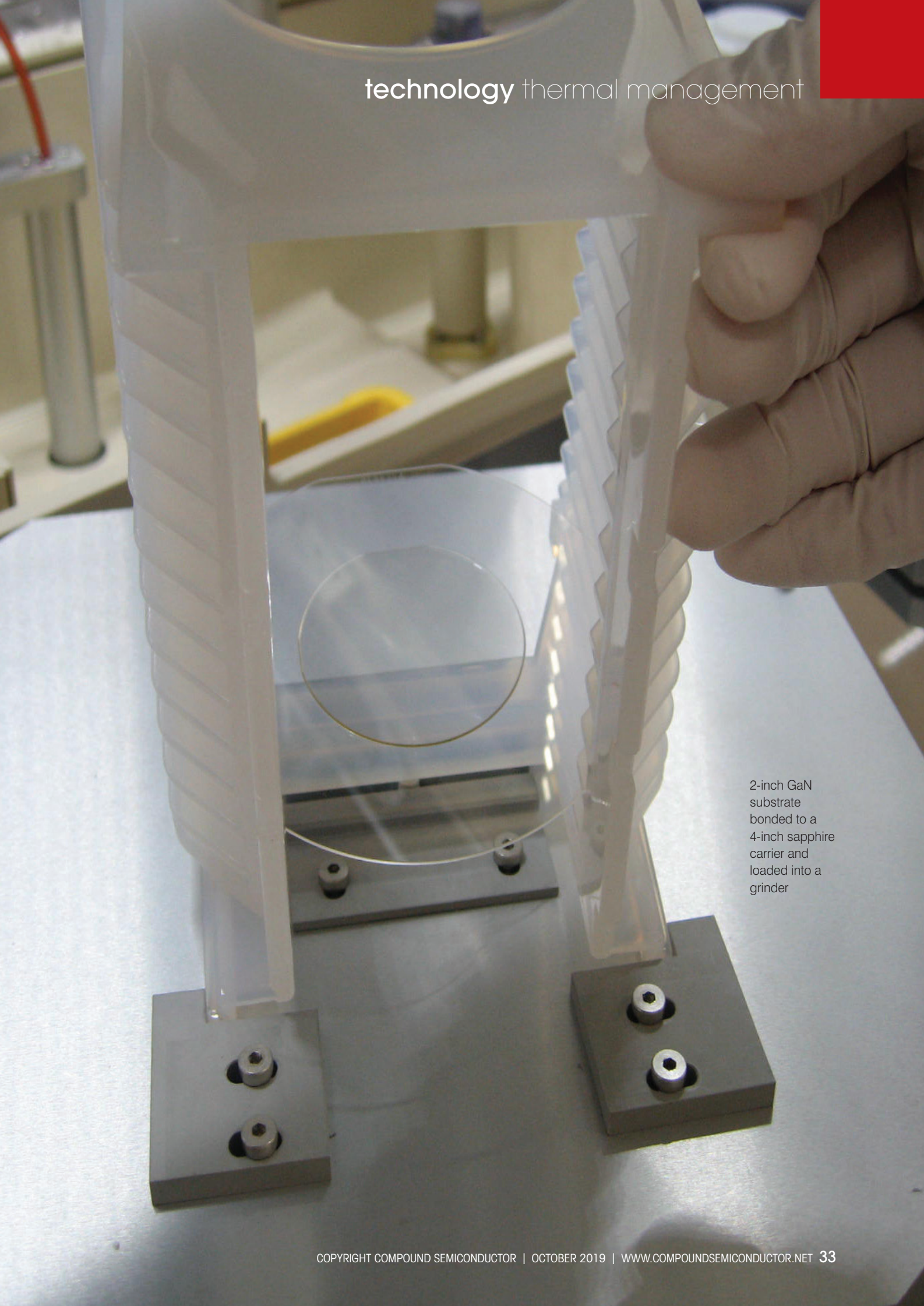
Until recently, switching to a GaN substrate has not been that attractive, due to its high electrical conductivity. But recently this has changed, now that iron-doping has enabled the production of semi-insulating GaN. Although substrates are small – their diameter is just 2-inch – they can reduce the extent of current collapse considerably.

The Achilles heel of the GaN substrate is its low thermal conductivity. At 230 W m^{-1} K^{-1}, it is almost half of that for SiC. This is a significant weakness, as it leads to a degradation of device performance and reliability. The problem is particularly acute when HEMTs are used for microwave heating, because this requires continuous operation of the device, and increases the extent of heat radiation.

Tackling this issue is our team from Fujitsu and Fujitsu Laboratories. Recently, using insights from thermal analysis, we have shown that backside processing can improve the thermal management of this device.

Thermal simulations

To optimise the thermal management of GaN-on-GaN devices, we begin by simulating a lateral HEMT with



2-inch GaN substrate bonded to a 4-inch sapphire carrier and loaded into a grinder

Table I. Comparison of substrates for GaN-HEMTs.

Substrate	Dislocation density of GaN epi-layer on sub. (cm^{-2})	Cost	Size	Thermal conductivity (W/mK)	Insulation
Sapphire	Not good (~10^9)	Good	6 inch (8 inch)	20	Excellent
Si	Not good (~10^9)	Excellent	> 8 inch	150	Not good
SiC	Good (~10^8)	Not good	4 inch (6 inch)	420	Excellent
GaN	Excellent (<10^6)	Bad	2 inch (4 inch)	230	Excellent

an output of tens of Watts. The merit of this approach, rather than an iterative one based on prototyping, is that it can quickly determine the best device structure and subsequent processes.

Before we started our simulations, we measured the thermal conductivity of semi-insulating GaN (0001) substrates grown using the void-assisted separation method by HVPE. Using the periodic heating method, we determined a thermal conductivity for the semi-insulating GaN substrate of 237 W m^{-1} K^{-1}. This value is in good agreement with recent measurements from other groups.

Our simulations considered a GaN epilayer on a native substrate, which has a backside coated with a layer of AuSn, attached to copper (see Figure 2(a)). In a HEMT, most of the heat is generated at the drain-side edge of the gate electrode, where the electric field concentration peaks. To try and replicate this scenario, we introduce heat sources, with dimensions chosen to match the gate electrode size. Each heat source has a power that is equivalent to a 10 W/mm HEMT, operating with an efficiency of 58.8 percent. We vary the width of these sources, but fix their length and height at 0.5 μm and 0.1 μm, respectively. In our simulations, these sources are placed on top of a GaN epilayer, and we vary the spacing between them, along with their number.

To ensure that our simulations are as realistic as possible, we account for the differences between growing GaN on its native substrate and on SiC. Growth of GaN-on-GaN ensures lattice matching, so there is no need for an AlN nucleation layer, and we can assume that the dislocation density in the GaN epilayer is as low as that in the GaN substrate. Based on these considerations, we adopt an extremely low value for the interfacial thermal resistance between the epilayer and the substrate – we use 1 × 10^{-10} m^2 K W^{-1} – and we set the thermal conductivity of the GaN epilayer to 230 W m^{-1} K^{-1}, which is approximately equal to that for the GaN substrate.

With GaN-on-SiC, simulations are markedly different. When GaN is grown on SiC, an AlN nucleation layer is often inserted between the buffer layer and the SiC substrate. Another key difference is that the

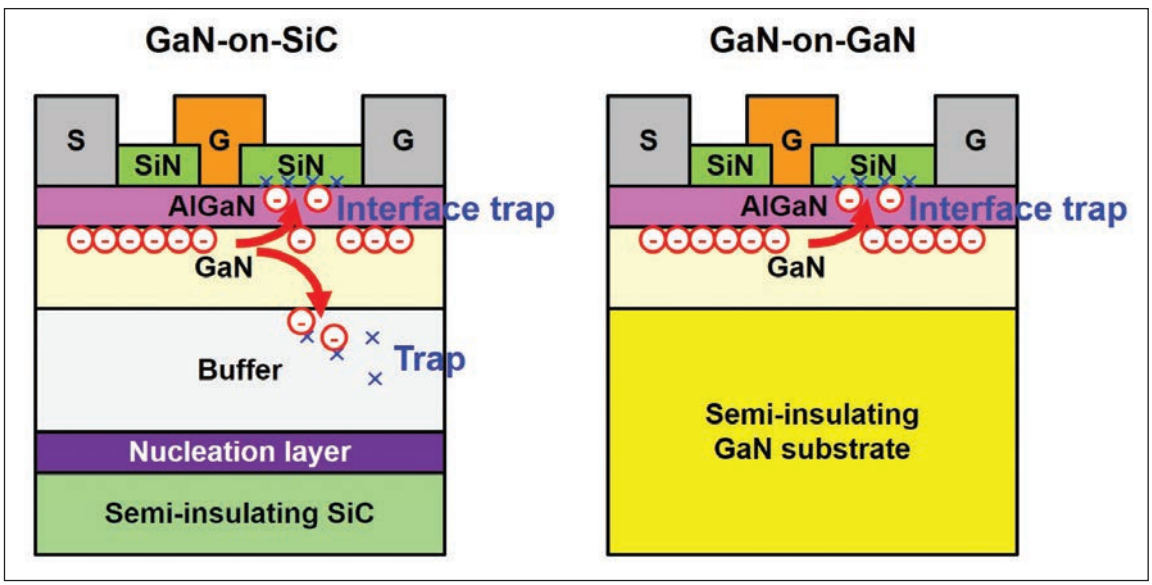


Figure 1. The cross-sections of typical GaN-on-SiC and GaN-on-GaN HEMTs.

dislocation density of the GaN epilayer is about two orders of magnitude higher than that of GaN-on-GaN. To capture all of this in our model, we select a much higher value for the interfacial thermal resistance – we use 2.5 × 10^{-8} $m^2 K W^{-1}$ – and we reduce the thermal conductivity of the GaN epilayer to 130 W $m^{-1} K^{-1}$. To determine the temperature rise, we calculate the difference between the maximum temperature of the simulated thermal distribution and the copper heatsink, held at 60 °C (see Figure 2 (b)).

We have found that for a heat source spacing of 30 μm, thinning the GaN substrate to just 100 μm minimises the temperature rise (see Figure 3(a)). Note, however, that as the width of the heat source increases, the temperature rise of GaN-on-GaN can overtake that for GaN-on-SiC. This indicates that GaN-on-GaN can be easily filled with heat.

Is this a concern? Although at first glance it would seem to be, we have demonstrated that GaN-on-GaN has a higher thermal management potential than GaN-on-SiC. When the heat source spacing exceeds 40 μm, the temperature rise for GaN-on-GaN is suppressed more than that for GaN-on-SiC (see Figure 3(b)).

To understand why this is the case, one needs to consider the heat transfer mechanisms at play. When heat sources are less than 30 μm apart, the heat that is generated interferes in the GaN epilayer. From here, heat transfers to the substrate and spreads in a direction parallel to the heat sources (see Figure 4(a)). In this case, a SiC substrate is preferable to one made from GaN, because it has a higher thermal conductivity.

A different conclusion is drawn when the spacing between the heat sources exceeds 40 μm. In this regime, thermal interference decreases, and it is effective to spread the heat in the GaN epilayer between the sources (see Figure 4(b)).

Where does the cross-over between the two modes of operation occur? Well, when the spacing between the heat sources is more than one-third of their width, GaN-on-GaN offers better heat dissipation than GaN-on-SiC, thanks to the higher thermal conductivity of the GaN epilayer.

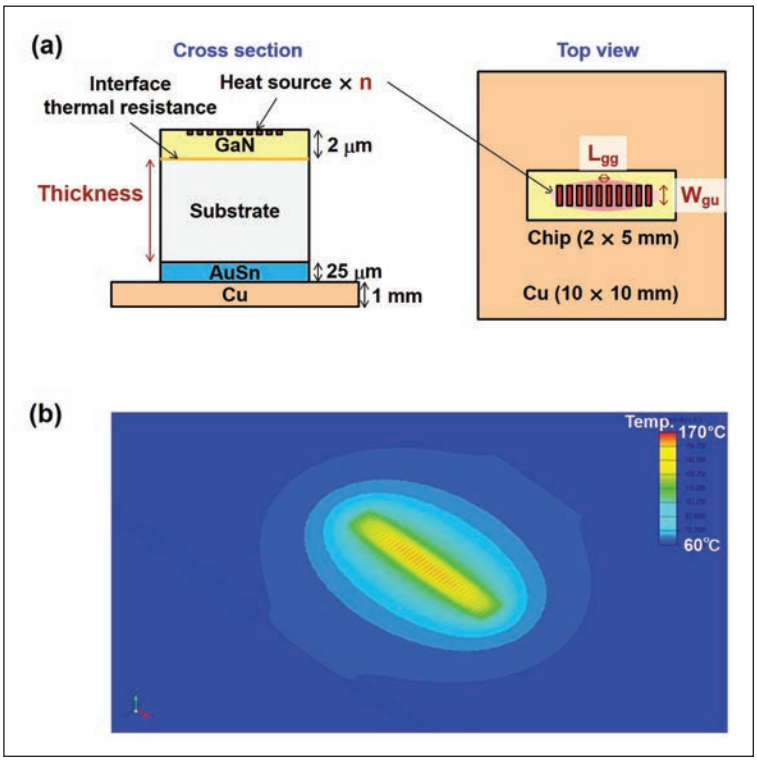


Figure 2. Simulated structure of a GaN-HEMT power amplifier (a) and an example of simulated thermal distribution (b).

This finding has implications for many different GaN-on-GaN architectures. It should influence those developing lateral GaN-on-GaN HEMTs, and also those making vertical GaN devices. These results have motivated our team to develop a GaN substrate thinning process, to aid heat dissipation in GaN-on-GaN HEMTs.

Backside processing

In general, GaN substrates are less sensitive to hardness than those made from SiC. Consequently, we can use our SiC through-substrate via-hole (TSV) process when backgrinding our GaN substrates. To undertake this, before we start backgrinding, we attach a 2-inch GaN substrate to a 4-inch sapphire support carrier with an adhesive (see the image on p. 33).

The results of our thermal simulations have led us to target a thickness for the processed GaN substrate of less than 150 μm. We realise this in two steps: we begin by using a coarse grinder, which removes

In general, GaN substrates are less sensitive to hardness than those made from SiC. Consequently, we can use our SiC through-substrate via-hole (TSV) process when backgrinding our GaN substrates

material at a rate of about 25 μm/min; and then we finish with a fine grinder, working at a rate of 1 μm/min. Using this approach, the total time for grinding is only about 15 minutes.

Backgrinding realised a target thickness of 145 μm and an excellent thickness uniformity – it was within ± 0.6 percent (see Figure 5). We processed three of these thinned wafers, a task that suggests that we have a stable, controllable process. Atomic force microscopy uncovered typical scratches in the surface. We found that at the centre of the wafer, the grinding marks are random, but at the top, these marks are aligned in one direction. Based on the scan of a 2 μm square, average surface roughness is less than 2 nm.

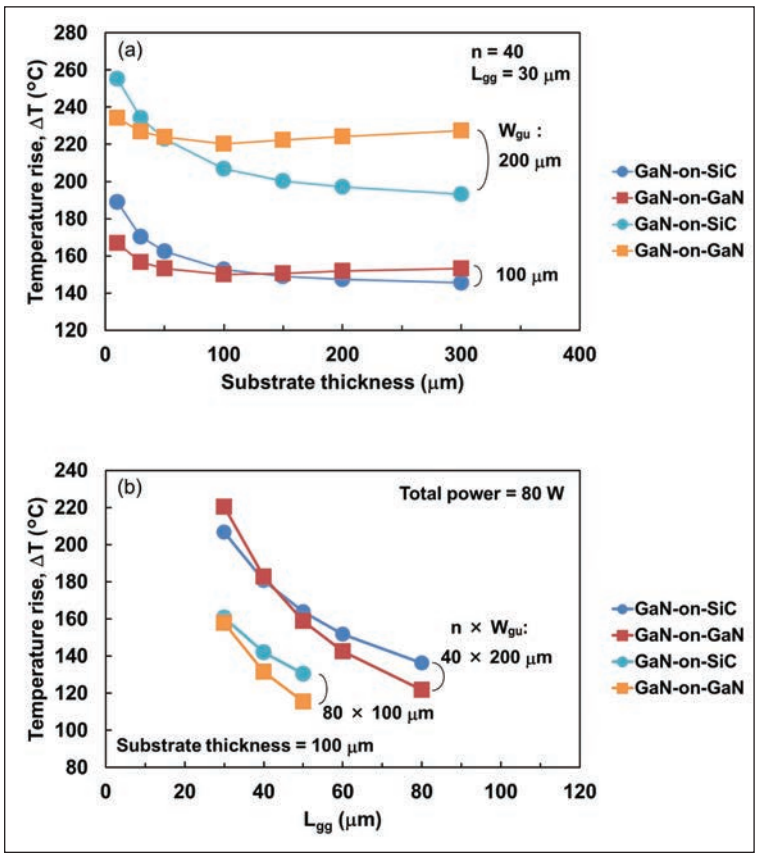


Figure 3. Simulated comparison of the temperature rise between GaN-on-GaN (▪) and GaN-on-SiC(•); (a)substrate thickness dependence, (b)gate-to-gate spacing distance dependence.

Unfortunately, backgrinding causes cracks in the wafer edges (see Figure 6(a)). This is an issue that never arose when grinding SiC. We attribute this problem to the GaN substrate being more brittle than SiC, and the wafer edge becoming knife-shaped, due to backgrinding. There is no cause for alarm, as we can eliminate the crack by trimming the wafer's edge.

To improve the finish of our backgrinded GaN, we use a chemical-mechanical polish. No scratch marks remain after polishing for 2 hours with a silica-based slurry. This process removed a further 10 μm of the GaN substrate (see Figure 5) and eradicated the wafer edge cracks (see Figure 6(b)). Polishing did compromise the thickness uniformity of the GaN substrate – it increased to just below ± 1.3 percent – but it is still sufficient for the task in hand. Of greater significance is the improved surface morphology, with average surface roughness slashed to just 0.2 nm or less (see Figure 7).

We also investigated a range of slurries. By refining our selection, we were able to trim the processing time by two-thirds. This time saving helps to reduce the time taken to produce GaN-on-GaN devices. In addition, we have recently increased our expertise, and can now control the thickness of the GaN substrate produced by backgrinding and chemical mechanical polishing down to 100 μm.

During the polishing process, we identified larger micropipes, with a typical diameter of 160 μm. Some

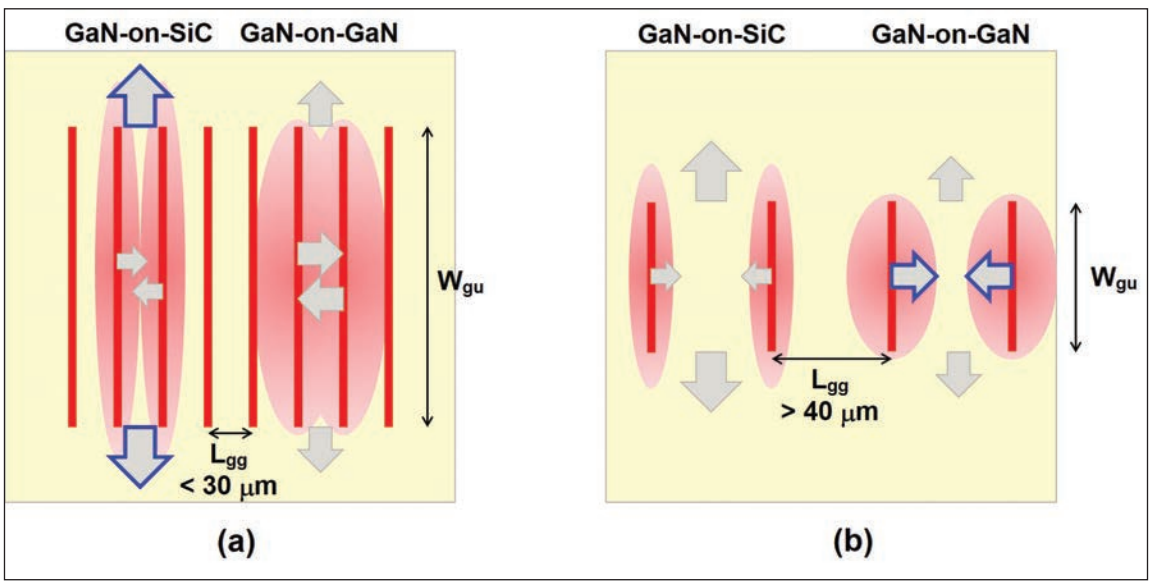


Figure 4. Difference in heat transfer mechanism, as viewed from the top of the device.

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of these result from the exposure of embedded micropipes by the polishing process. However, the majority originate from polishing itself, which causes an expansion of dislocation defects. In the GaN substrates that we use in this work, the dislocation density is less than 5×10^6 cm^{-2}. Going forward, this figure should fall, leading to fewer micropipes, because manufacturers of GaN substrates are striving to make better, lower-cost, larger material.

Future plans

One of our goals is to evaluate the thermal dissipation of the GaN-on-GaN HEMT for a substrate thickness that has been optimised by simulation. Note, though, that when designing the layout of the device, it is important to consider not only the thermal characteristics of this transistor, but also its high frequency performance.

The interplay between these two is not trivial. One option to suppress the temperature rise is to reduce the gate width, a move that also allows improvement in high-frequency characteristics through a reduction in phase rotation. Another way to reduce the rise in temperature is to put the gates further apart, but this degrades the high-frequency performance, due to an increase in the phase shift.

To improve the high-frequency characteristics of GaN-on-GaN HEMTs, we have started to develop GaN TSVs. This modification decreases source inductance, but possibly at the expense of a compromise in heat transfer. Conventional TSVs tend not to be completely filled with metal, and they contain cavities. The details of their design and placement must be taken into account when considering heat transfer and the high frequency characteristics of the HEMT.

Additional gains in heat dissipation can be realised through the introduction of a diamond heat spreader. This is very effective, due to its extremely high thermal conductivity of 2000 W m^{-1} K^{-1}. We are pursuing this approach, and have already succeeded in bonding a GaN substrate to diamond using an atomic diffusion bonding process developed by Takehito Shimatsu's group at Tohoku University, Japan. This breakthrough dramatically improves heat dissipation in GaN-on-GaN devices.

This research was partially supported by the Japan Ministry of the Environment as part of the project Technical Innovation to Create a Future Ideal Society and Lifestyle.

Further reading
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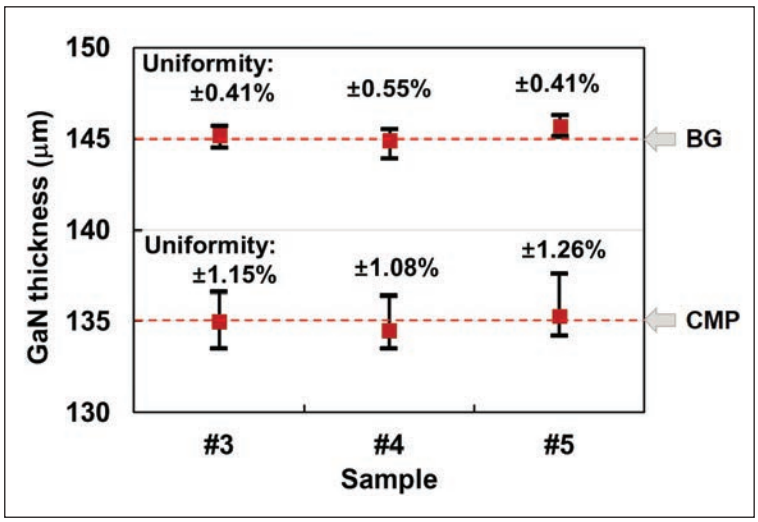

Figure 5. Thickness of the three processed GaN substrates after backgrinding (BG) and chemical-mechanical polishing (CMP).

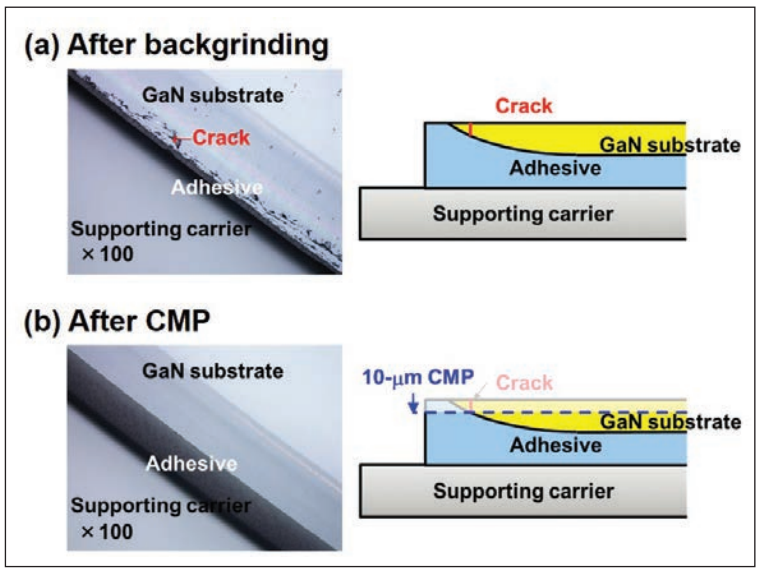

Figure 6. Photograph and schematic cross-section of wafer edge after backgrinding (a) and chemical-mechanical polishing (CMP) (b).

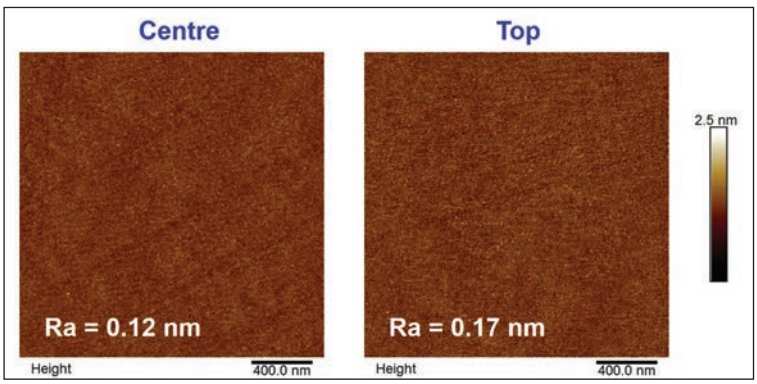

Figure 7. Atomic-force microscopy images of a GaN substrate after chemical-mechanical polishing.

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Stepper streamlines pHEMT production for 5G markets

Introducing a 248 nm stepper enables highly uniform high-yield manufacture of miniaturised pHEMTs

BY BARRY LIN, CHAO-MIN CHANG AND CLIFF YANG FROM WAVETEK MICROELECTRONICS CORPORATION

Caption Left: xxx

THE ROLL-OUT of the 5G network is now underway. So, if you are lucky enough to live in an area where it has just been deployed, you will have the opportunity to tap into high data rates transmission and an increase in service capacity. Additional merits of 5G include an ultra-low latency – it is in the millisecond range – that will enable a variety of new applications that were not possible with its predecessor, such as widespread implementation of autonomous vehicles and real-time industrial connectivity.

In order to fully utilise the key features within 5G communications, several bands within the millimetre-wave range have been allocated for this purpose (see Figure 1). Actual band allocation varies from country to country, depending on what is available and what can be re-allocated, but in general, the ranges from 24.25 GHz to 29.5 GHz and 37 GHz to 43.5 GHz are the most promising frequencies for the early deployment of 5G millimetre-wave systems.

Several technologies are vying for success in these millimetre-wave bands. One is advanced RF CMOS processes that could be used for handset applications. Today, circuits with features at the 20 nm or 22 nm node are often used to design integrated front-ends, which include a low-noise amplifier, switch, and PA. Another option is the advanced GaAs pHEMT. In the form of an enhancement-mode pHEMT with a 0.15 μm gate length, it offers a lower noise figure and a higher power efficiency than its CMOS rival, and is comparable or better in other regards (see Table 1 for details).

Superiority of the DUV stepper

The traditional method for realising a pHEMT with a 0.15 μm gate length or less is electron-beam lithography. However, this technique has a low throughput and a high cost, compromising high volume production.

To address these weaknesses, our team at Wavetek Microelectronics Corporation (WTK), a UMC subsidiary, is using the advanced photolithography technology of our parent company. Drawing on this enables us to be the leading commercial GaAs foundry employing a deep-UV stepper. We use this to define 0.15 μm gates in E-mode pHEMTs in a high-volume production environment. This makes our pHEMT technology, produced with a KrF 248 nm stepper, one of a handful of viable candidates for future 5G millimetre-wave MMICs, which must be manufactured using mature, high-volume, low-cost production capabilities.

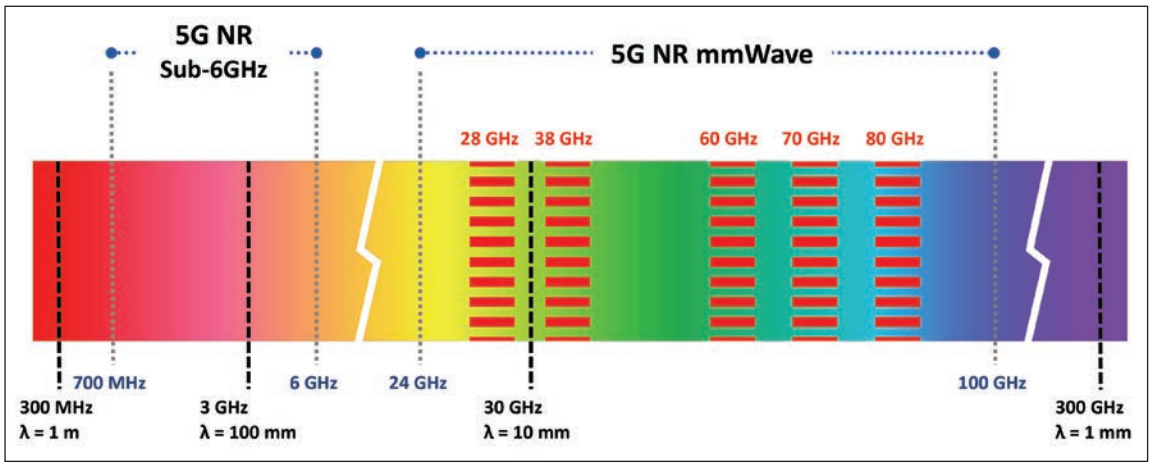

Figure 1. Electromagnetic spectrum for 5G communications

Either MBE or MOCVD can be used to form the heterostructures for pHEMTs, which feature a high-mobility conduction channel created from a two-dimensional electron-gas. On these epiwafers we add drain/source ohmic contacts, formed from an AuGeNi alloy, and a mushroom-shaped Schottky gate, also known as a T-gate (see Figure 2). This gate, created on top of a recess-etched trough, holds the key to forming high-quality, enhancement-mode pHEMTs. The recessed gate region has to be critically etched to ensure a uniform threshold voltage distribution across the wafer, and control wafer-to-wafer reproducibility.

We are not the first to turn to stepper technology for the production of compound semiconductor devices. For gates with lengths of 0.25 μm or more, i-line steppers have been used for several decades. But this form of stepper cannot define dimensions of 0.15 μm and below, a domain that is traditionally only associated with direct-write electron-beam lithography. This technique offers flexibility, as it is able to switch between multiple products, but it is limited to smaller volume production.

To realize cost-effective, high-volume production of MMICs with a 0.15 μm pHEMT technology within a 6-inch GaAs foundry, we have turned to a deep UV stepper (a typical device, imaged with a scanning electron microscope, is shown in Figure 3). High-volume production commenced in 2018, and at this year's IMS meeting, we generated significant attention when we unveiled this production ready technology to our peers.

A key characteristic of any pHEMT is its threshold voltage. For our enhancement-mode device, it's about 0.3 V. To determine the degree of uniformity, we have mapped one of our processed wafers with a probe. Results indicate that the standard deviation is just 13 mV (see Figure 4), a value comparable to our 0.25 μm pHEMT technology produced with a standard i-line stepper. The high degree of uniformity highlights the excellent gate threshold voltage controllability of our deep-UV stepper lithography process and our gate-etching process.

Extensive evaluation

To evaluate the yield enhancement provided by our new process, we have used a test vehicle mask to make more than 200,000 discrete, depletion-mode pHEMTs from a 6-inch wafer. A chip probing test reveals the tightly controlled distribution of drain leakage current (see Figure 5). These measurements were made on D-mode pHEMTs, which have a median pinch-off voltage of -0.7 V, at a drain voltage of 4 V and a gate voltage of -1.3 V – that's 0.6 V deep into the sub-threshold region. The very small variations

Table 1. Key parameter comparison between 0.15 μm. E-pHEMT (ED15-01) and 22 nm SOI CMOS(22FDX). Data taken from Hoentschel *et al.*, ISTE OpenScience, pp. 6, London, UK, 2019.

Items		22FDX [Ref. 1]	ED15-01
Vds [V]		0.8	5
BVgd [V]		-	12
f_T [GHz]	n-FET	347	100
	P-FET	275	
f_{MAX} [GHz]	n-FET	371	320
	p-FET	299	

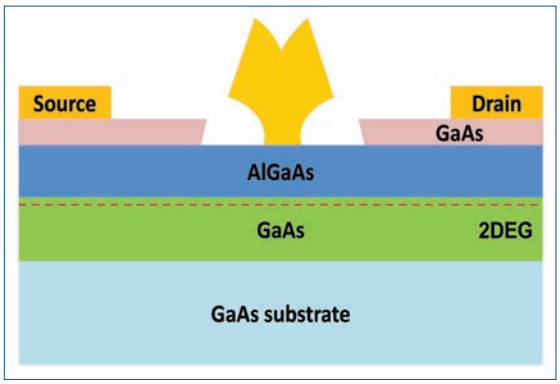

Figure 2. A typical E-mode pHEMT.

in the sub-threshold leakage current underscore the tightly controlled threshold voltage. With the new process, wafer yield exceeds 98 percent.

Measurements on one of our E-mode pHEMTs with four 75 μm gate fingers reveal that at a gate-source voltage of 0.9 V, the drain-source current is 400 mA/mm, while the maximum extrinsic transconductance is 880 mS/mm at a gate-source voltage of 0.72 V (see Figure 6). Additional investigations show that the drain-to-gate breakdown voltage exceeds 12 V, the typical cut-off frequency is 100 GHz, and the maximum oscillation frequency is more than 300 GHz.

We have plotted the maximum oscillation frequency as a function of gate voltage at different values of drain bias (see Figure 7). Realising a high maximum oscillation frequency at a high breakdown voltage highlights the great potential of our technology to serve in 5G millimetre-wave communications all the way up to 43 GHz, even with a 5 V power supply.

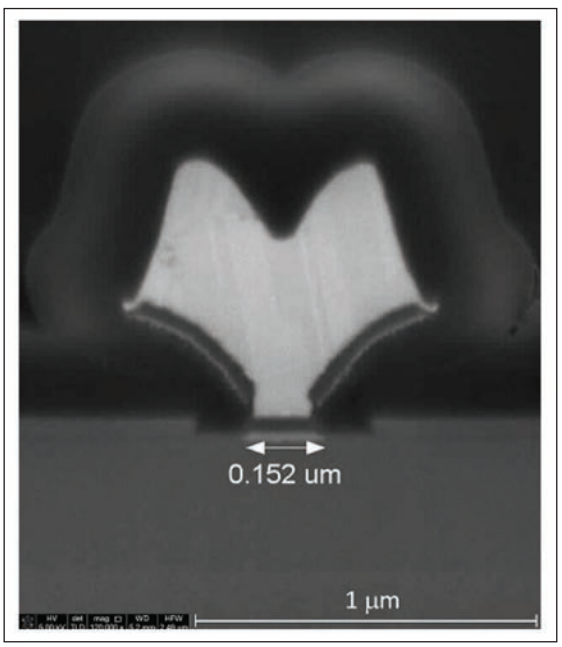

Figure 3. A scanning electron microscopy cross-section image of 0.15 μm gate defined by deep UV stepper photolithography.

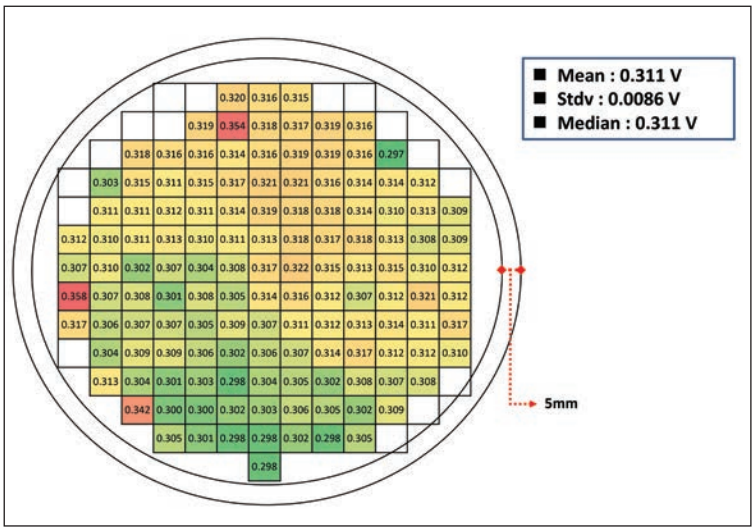

Figure 4. The threshold voltage wafer map of a typical 0.15 μm E-pHEMT device over a 6-inch wafer.

A key requirement for a receiving-end, low-noise-amplifier is a low noise figure. We have conducted a frequency sweep, uncovering the noise figures for an E-mode device with four 75 μm gate fingers. Tests at 12 GHz, under a drain source bias of 3 V and a drain-source current of 10.8 mA, reveal a minimum value for noise of just 0.42 dB and an associated gain of 10.5 dB (see Figure 8). Increasing frequency to 40 GHz produces an increase in noise to 1.27 dB, and trims the associated gain to 5.18 dB. Note that noise is below 1dB at 28 GHz, for a drain-source voltage of 3 V and a current density of 36 mA/mm.

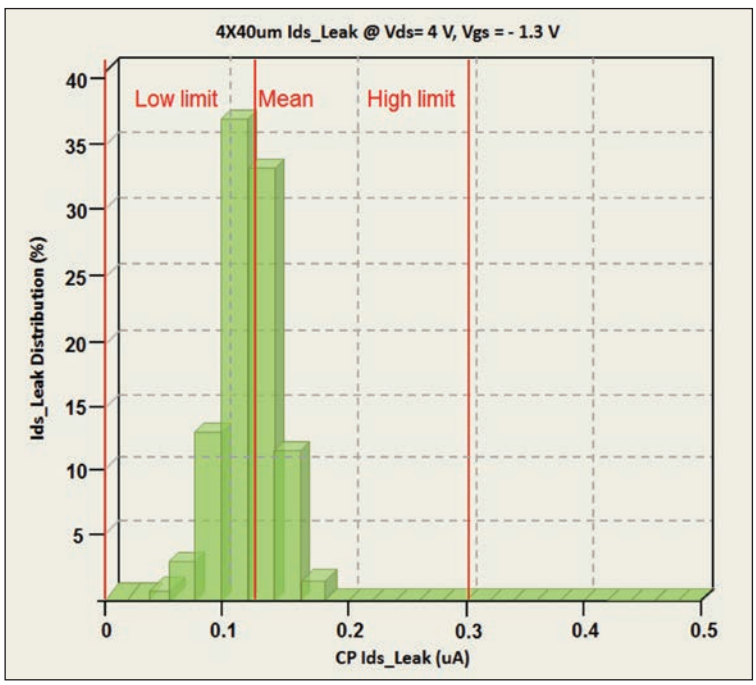

Figure 5. A histogram of a tightly controlled sub-threshold drain current (Ids_Leak) in a 0.15 μm D-pHEMT device used in WTK's technology development.

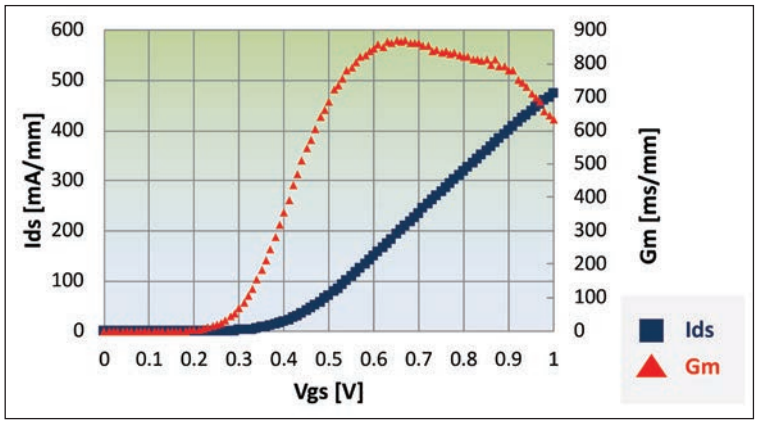

Figure 6. A DC transfer curve of WTK's 0.15 μm E-pHEMT with gate fingers of a four by 75 μm device.

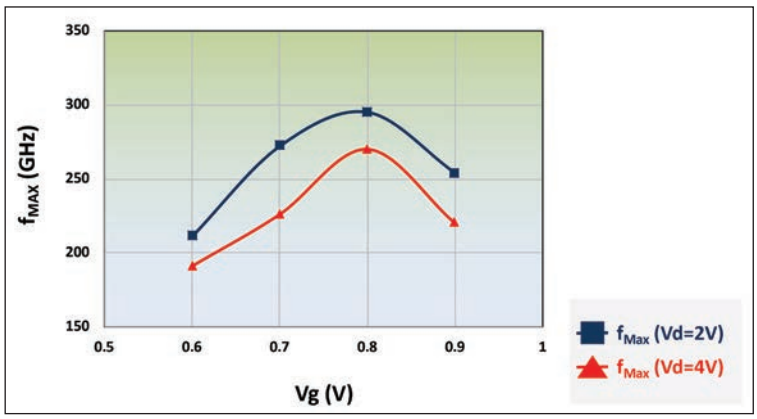

Figure 7. A typical f_{MAX} vs. V_g plot at different V_{ds} of WTK's 0.15 μm E-pHEMT.

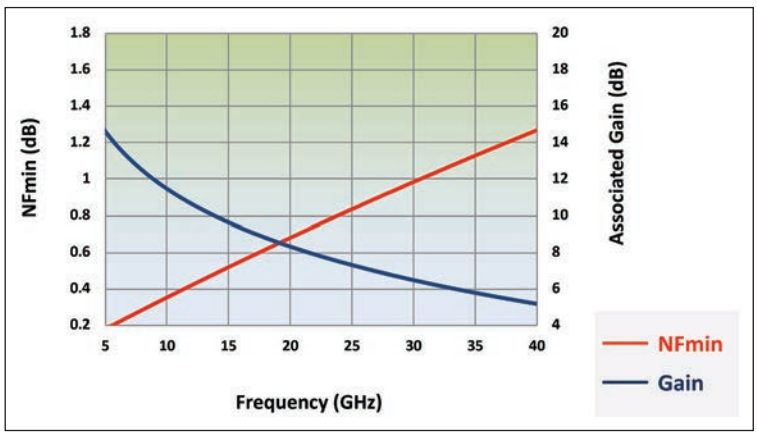

Figure 8. A frequency sweep of noise characteristic of WTK's 0.15 μm E-pHEMT.

To verify the RF power performance of our 0.15 μm E-mode pHEMT processed with the deep UV stepper, we have designed and produced a one-stage common source power amplifier. It features a transistor with four 75 μm gate fingers to provide the amplification, and several series and shunt transmission lines to match input and output networks. The capacitors are adopted for DC block and bypass networks.

Our power amplifier draws a 60 mA quiescent DC current from a 5 V supply voltage. Power sweeps show that the saturation output power is 22.2 dBm, and the peak power-added-efficiency hits 50 percent at 30 GHz. Power density tops 553 mW/mm, providing further proof that our 0.15 μm technology can provide a good platform for demanding millimetre-wave circuit designs.

Today, all 5G millimetre-wave handset PAs are demonstrated in advanced CMOS technology, thanks to its higher integration with CMOS RF front-end and controller circuits in an adaptive array configuration. However, the node required for operation at this frequency has a low breakdown voltage, and a stacking approach involving more than three levels is needed to produce a PA with sufficient output.

Unfortunately, there are downsides to stacking. The effective maximum oscillation frequency tumbles, limiting key high-frequency performance characteristics, such as power density and power-added efficiency. The upshot is a hike in power dissipation and a dramatic decline in power performance, limiting the operating distance of the handset. To address these issues, we advocate a heterogeneous integration approach, combining a CMOS front-end chip with a controller and a high-efficiency, high-power-density pHEMT PA chip. When it comes to selecting the PA, we believe that our 0.15 μm E-mode pHEMT technology is very competitive. Produced with a deep UV stepper, it offers an affordable, high power density, high power-added efficiency solution to address future 5G communications requirements in millimetre-wave bands.

Further reading

J. Hoentschel *et al.* ISTE OpenScience, pp. 6, London, UK, 2019
C-M. Chang *et al.* 2019 International Conference on Compound Semiconductor Manufacturing Technology Digest, pp. 333-336, May 2019.
T. Lodhi *et al.* Compound Semiconductor IC Symposium, 2006
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M. M. Abdin *et al.* 2017 IEEE 18th Wireless and Microwave Technology Conference, 2017

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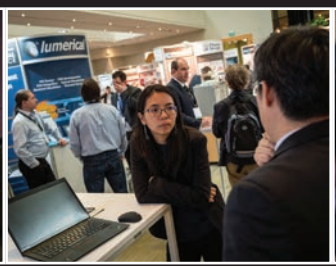



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Supercharging the HEMT

Cranking up the aluminium content in the AlGaN channel promises to create high-power HEMTs for extreme operating conditions.

BY PATRICK CAREY, FAN REN AND STEPHEN PEARTON FROM THE UNIVERSITY OF FLORIDA AND ALBERT BACA, BRIANNA KLEIN, ANDREW ARMSTRONG ANDREW ALLERMAN AND ROBERT KAPLAR FROM SANDIA NATIONAL LABORATORIES

POWER ELECTRONICS ARE UBIQUITOUS. They are deployed in satellites, unmanned autonomous vehicles, electric cars, photovoltaic systems, and power transmission on the utility grid.

Silicon is still the dominant material for making these power devices, but in the last decade or so there has been an increasing use of wider bandgap materials, such as SiC and GaN. This move has much merit: it opens the door to higher switching frequencies and superior thermal management; and it slashes the size and weight of the power converter, by allowing the use of smaller, lighter passive elements while simplifying thermal management.

The introduction of SiC and GaN devices is not going to be the end of the story, but the beginning of a journey to materials with even wider bandgaps. Under development right now are devices made from ultra-wide bandgap semiconductors, such as diamond, Ga_2O_3, BN and high-aluminium-content AlGaN. This class of materials promises to propel device performance to a new level.

In applications where devices are deployed in an extreme environment, high powers have to go hand-in-hand with greater robustness. These attributes may be required in avionics, automotive, nuclear, defence, and extra-terrestrial applications. For example, in exploratory missions to the surface of Venus, devices must withstand temperatures of 500°C, while maintaining their performance in corrosive sulfuric acid clouds. In addition, there can be the need to provide continuous operation when bombarded by radiation. The Galileo orbiter, which probed Jupiter for many years, withstood an irradiation dose above 600 krad before it plunged to its planned demise as the effects of radiation damage became unrecoverable.

Traditionally, it has been the wide bandgap materials SiC and GaN, working in conjunction with other technologies, that have provided a reasonably successful approach to extending device lifetimes in these high-power applications operating in extreme environments. But these materials are beginning to reach maturity, so obvious questions arise. Two that top the list are: What is the next material system for power electronics? And what will be the next innovation?

Every ultra-wide bandgap semiconductor has its pros and cons. Often there are concerns related to cost, substrate availability, and existence of controlled doping and contact schemes. For example, while Ga_2O_3 has made some progress in vertical diodes with bulk growth technology, its low thermal conductivity, lack of native *p*-type doping, and low electron mobility are drawbacks for its use in power electronics.

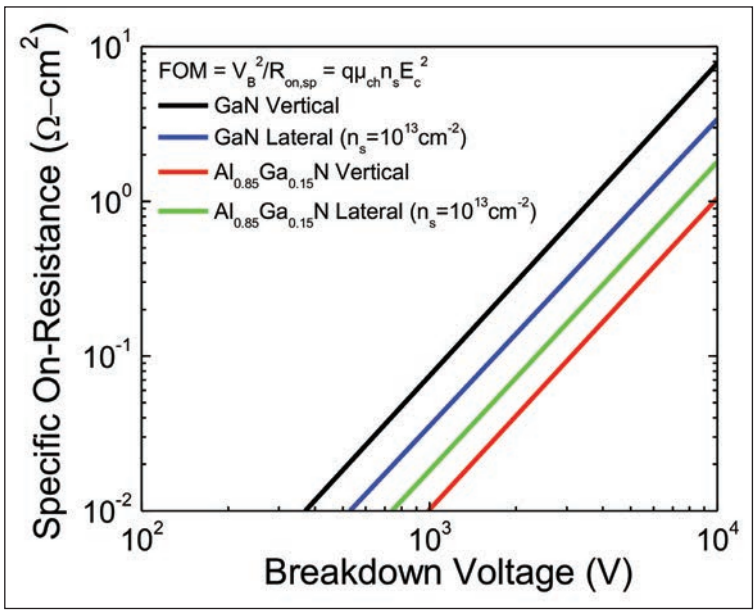


Figure 1. Specific on-resistance versus breakdown voltage for high-aluminium-content devices compared with GaN.

An attractive option is to build on the success of previous efforts. That's possible with GaN, a material that has benefitted from more than thirty years of exploration and investment. Its performance can be improved by increasing the aluminium content in the AlGaN channel of the HEMT. That's the approach trailblazed by our team, a partnership between the University of Florida and Sandia National Laboratories.

One of the greatest strengths of AlGaN is its ultra-wide bandgap, which leads to a very high critical breakdown field, E_c. The exact relationship between the critical field and the bandgap, E_g, is a focus of active research, but it is essentially a power law, with E_c proportional to $E_g^{2.5}$. Due to this relationship, when the aluminium content increases to 70 percent or more, the bandgap widens to 5.4 eV, and the breakdown voltage increases – it should hit 13.4 MV/cm (see Figure 1 for a comparison of aluminium-rich devices and those with pure GaN, illustrating the potential for devices that combine an ultra-low specific on-resistance with a high breakdown).

Like other ultra-wide-bandgap materials, alloys of aluminium-rich AlGaN hamper the production of low-resistance ohmic contacts. In addition, with this ternary it is challenging to realise meaningful carrier concentrations and high mobilities. However, excellent progress has been made to date in all these areas.

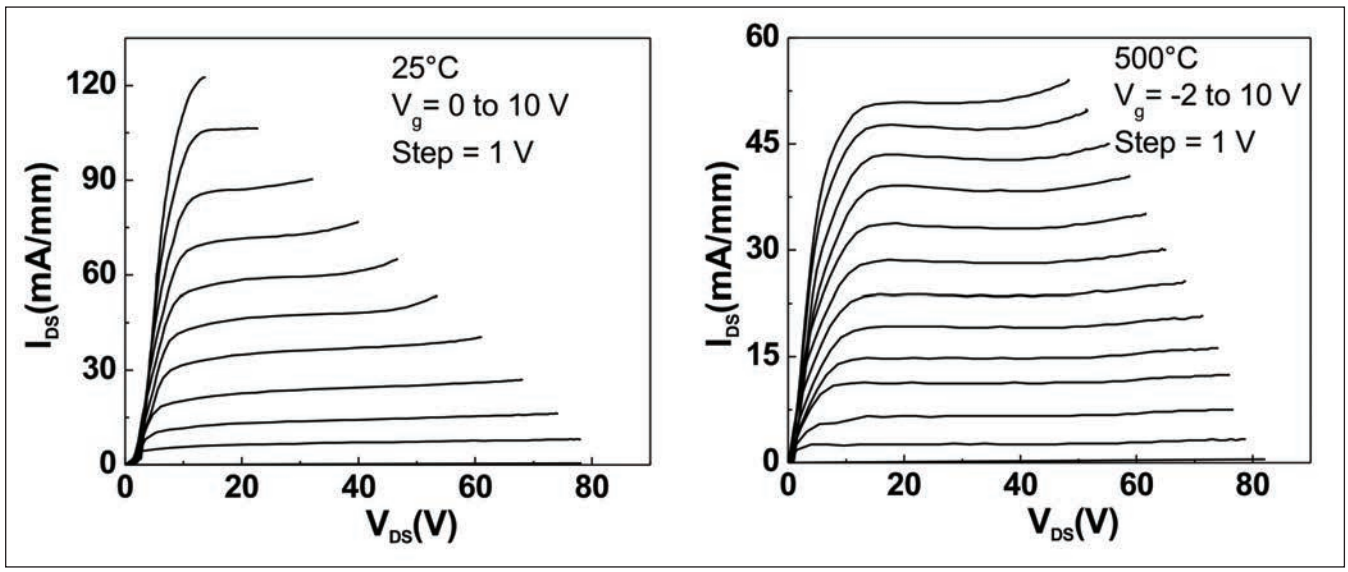
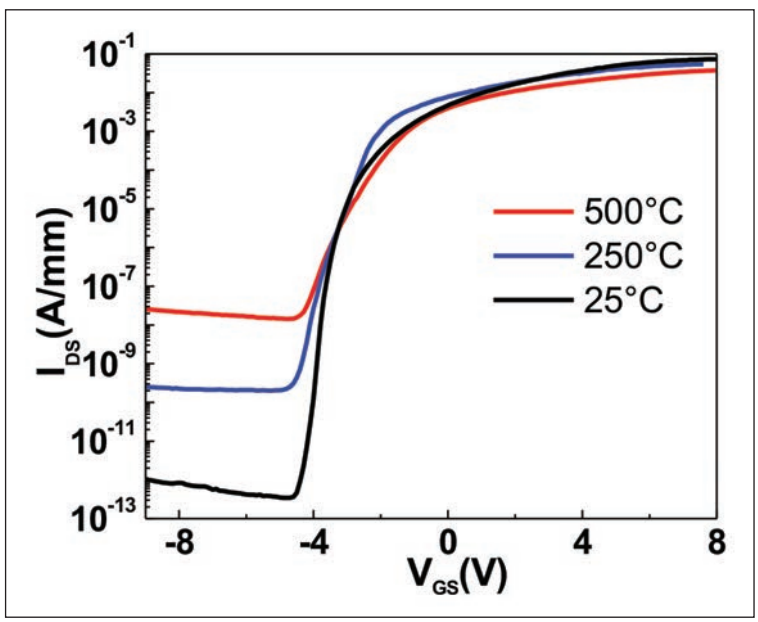


Figure 2. Typical current-voltage characteristics at 25 °C and 500 °C.

Encouragingly, initial irradiation studies on HEMTs with high-aluminium-content AlGaN-channels show that bombardment with 2.5 MeV protons has little effect on this device. However, research prototypes show a reduced single-event burnout tolerance in simulated space environments.

These results indicate that there is an improvement in total dose irradiation hardness when moving from a GaN-channel device to an AlGaN HEMT. This is to be expected, given the strength of the atomic bonds. For GaN, it is 8.92 eV/atom, while for AlN, it is 11.52 eV/atom – to put those figures in context, values for silicon and GaAs are just 2.34 eV/atom and 2.17 eV/atom, respectively.

Figure 3. I_d-V_{gs} curves at select temperatures from 25 °C to 500 °C.



Growing AlN

For every compound semiconductor, it is ideal to grow the epilayer on a native substrate. So, for AlN HEMTs, the perfect platform is high-quality, single-crystal AlN. This foundation has a bandgap of 6.2 eV, a high thermal conductivity of 285 W m^{-1} K^{-1}, and it provides a nearly lattice-matched substrate for aluminium-rich AlGaN epilayers, greatly reducing strain and threading dislocation density in this ternary.

Producing high-quality AlN substrates is very challenging. The most promising method for preparation, physical vapor transport, produces material with dislocation densities below 10^3 cm^{-2}. However, commercialising substrates with this technique is far from easy, as it is tricky to combine a sufficient size with a low defect density.

Due to the high cost of AlN substrates, the majority of efforts directed at developing AlGaN are undertaken with sapphire or SiC substrates. They provide a template for growing a layer of AlN, which provides the foundation for AlGaN devices.

Growing AlN on sapphire is not straightforward. Two of the greatest issues are the large lattice and thermal conductivity mismatches. Failure to take sufficient care leads to cracks developing in AlN grown on sapphire after the critical thickness has been reached, due to tensile stress from the coalescence process.

Much effort has been devoted to avoiding this, and after 15 years of detailed study of the epi-growth of AlN epilayers on sapphire, there are now several reports that detail different growth processes for producing device-quality AlN epilayers.

When AlGaN epilayers are grown on AlN-on-sapphire templates, it is the composition of the AlGaN that determines epilayer, lattice and thermal mismatch. These mismatches can be exacerbated between the AlGaN and AlN. To reduce the stress and the density of defects in AlGaN epilayers, engineers can turn to compositionally-graded layers or superlattices, or begin by intentionally inducing three-dimensional growth modes, before switching to two-dimensional

growth for planarization.

Processing challenges

Our team has used MOCVD to produce aluminium-rich AlGaN HEMTs on sapphire. The typical composition for these structures is a 85 percent aluminium barrier layer and a 70 percent aluminium channel layer. We refer to this structure as 85/70.

With these compositions, the epilayers can behave as insulator-like materials, hampering the formation of ohmic contacts. Regardless of metallisation and annealing temperature, it is difficult to achieve linear, low-resistivity contacts without employing more advanced techniques. Our simple planar contacts have realised a contact resistivity of 2×10^{-2} Ω-cm^2. While this resistivity is still far higher than 10^{-6} or less, a typical range of values that are easily achieved in GaN devices, we believe that it is quite reasonable for an early attempt with our new aluminium-rich materials.

One established process for the AlGaN HEMT is plasma etching, a technique that is widely used with GaN. It is relatively easy to etch tens of nanometres per minute, a rate that optimises the control of the recessed gates. There is a danger that surface roughness can arise from micro-masking of the surface of Al_2O_3. However, this can be prevented with an appropriate gas chemistry to produce surfaces with a root-mean-square roughness below a nanometre. We have found that a small addition of BCl_3 assists in the removal of Al_2O_3, to yield a better surface than that realised with a pure Cl_2/Ar environment.

Trumping GaN

We have evaluated the performance of our 85/70 transistor from room temperature up to 500°C. Measurements of the forward current as a function of voltage reveal full gate modulation across the entire temperature range (see Figure 2). A great attribute of these devices is that they produce full pinch-off up to these temperatures. In sharp contrast, GaN HEMTs fail to provide full pinch-off above 300 °C – and they are plagued by a poor current on/off ratio, which is typically around 10^4.

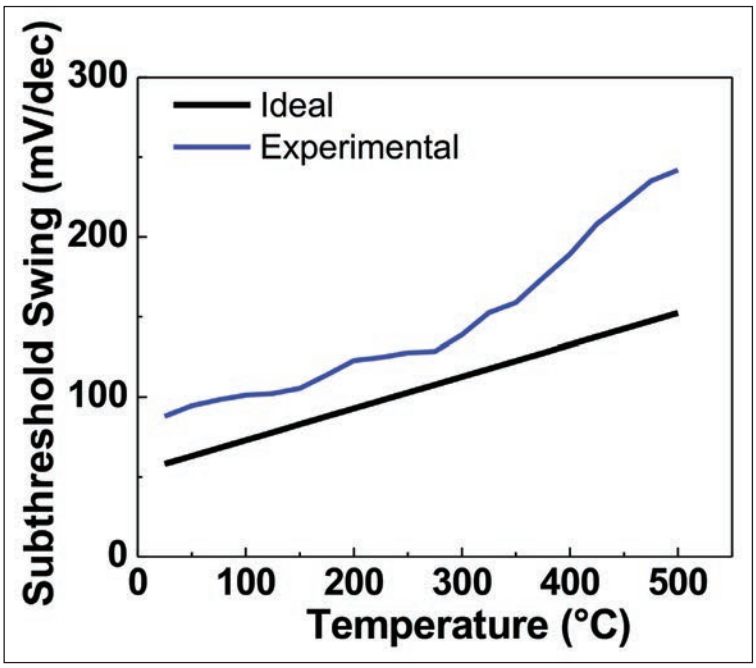


Figure 4. Experimental and ideal subthreshold swing as a function of temperature.

One characteristic of SiC and GaN devices is a current-voltage curve with an upward slope in the saturation regime at elevated temperatures. This behaviour is not ideal – the slope should be horizontal – and it indicates a low output resistance, which hinders high-temperature performance. The is not an affliction for our 85/70 devices, which have a reasonably horizontal current-voltage slope in the

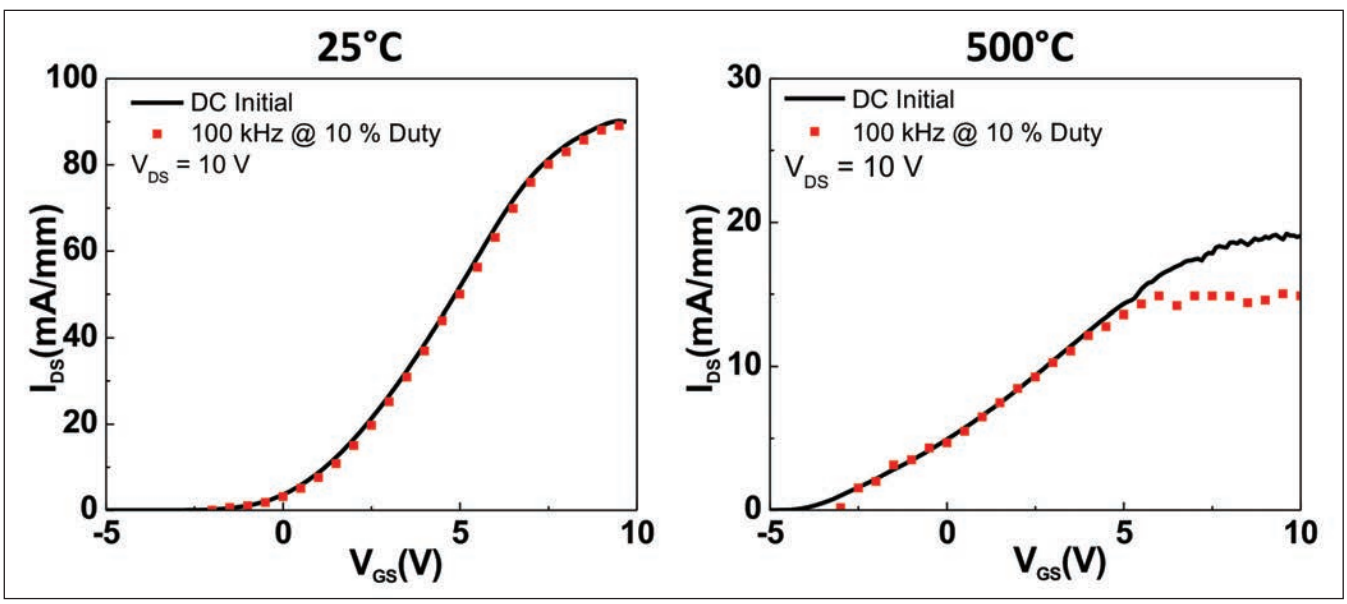


Figure 5. Gate lag at 25 °C and 500 °C performed at 100 kHz, 10 percent duty, and a drain-source voltage of 10 V.

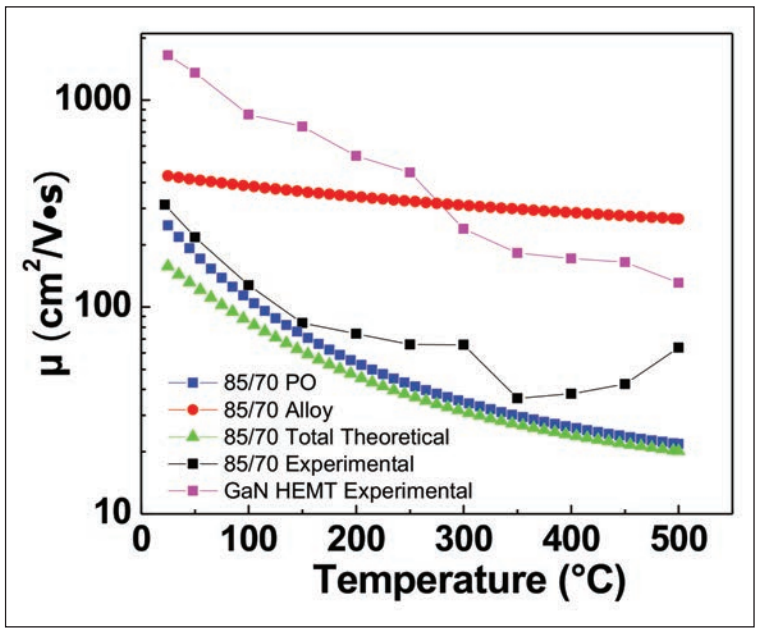


Figure 6. Modeled and experimental electron mobility as a function of temperature for the 85/70 HEMT, compared with a traditional GaN HEMT.

saturation regime at 500 °C. This unique performance provides a significant improvement over traditional GaN-channel HEMTs.

At very high temperatures, the quality of the gate dictates channel modulation characteristics. We have undertaken initial studies with a Ni/Au gate. At room temperature, the Schottky barrier height is a moderate 1.2 eV, a value comparable to that of a GaN HEMT at room temperature. Raise the temperature, however, and device performances diverge. For our 85/70 device, the barrier height of the gate appears to be entirely unpinned, with a magnitude increasing to 3.3 eV at 500 °C. The lack of pinning is highly desirable, as it implies that the electrons on the gate gain thermal energy under heating, while in tandem the barrier height increases in magnitude, preventing an excessive leakage current at high temperatures. Another advantage of the high Schottky barrier is that it allows AlGaN devices to be driven at higher current densities and at higher drain voltages than GaN equivalents. The level of superiority is particularly acute at elevated temperatures.

It is worth noting that the unpinned behaviour may not hold true for other gate metal stacks. We are investigating this as we explore different designs to further improve device performance.

A significant benefit that stems from turning to high-aluminium-content AlGaN is the increase in breakdown performance. Efforts by our team reveal that AlGaN HEMTs are capable of withstanding electric fields up to 2.5 MV/cm, a figure that is approaching the SiC limit. Far higher values may be possible, as we are yet to employ techniques to improve performance, such as a source field plate, and it is still early in the development of this material system. For example, we have not yet begun to explore better dielectrics to match the breakdown field of AlGaN. Our hope is that as the growth, the device design, and the processing are optimised over the coming years, fabricated devices will move closer to the theoretical limit of 13.4 MV/cm.

Better breakdown characteristics are very valuable, as they drive down the power loss of the device that is associated with the reverse leakage current. For our devices, the current is as low as 10^{-12} A/mm at room temperature, rising to just 10^{-8} A/mm at 500°C (see Figure 3).

These plots of reverse leakage at different temperatures can be used to determine an activation energy, and ultimately the mechanism behind the drain leakage current. Using an Arrhenius plot, we have determined an activation energy of 0.63 eV for temperatures below 350 °C, and an activation energy of 0.076 eV above 350 °C. An activation energy of 0.63 eV is consistent with Poole-Frenkel emission, while that at 0.076 eV is associated with band-to-band tunnelling. This can take place at this low energy due to significant bending within the conduction and valence bands.

The other key metric that can be extracted from these current-voltage plots is the sub-threshold swing. At room temperature, our devices have a value of 80 mV/dec, not far from the ideal 60 mV/dec (see Figure 4).

From these graphs of sub-threshold swing we are able to extract the interfacial trap density. It is clear that there are two distinct linear regions: one from

One envisioned use for our aluminium-rich AlGaN HEMT is high-power switching. To investigate its potential, we have undertaken gate switching at 100 kHz and a 10 percent duty cycle, using a constant drain bias of 10 V. These measurements reveal a near-ideal pulsed current across the entire temperature range

25 °C to 300 °C, associated with trap densities of 2×10^{11} cm^{-2}; and the other from 300-500 °C, for trap densities of 3×10^{12} cm^{-2}. These values are very encouraging, suggesting that the interface in our devices might even be better than that in AlGaN/GaN, which has a typical trap density on the order of 10^{12} cm^{-2} at room temperature.

One envisioned use for our aluminium-rich AlGaN HEMT is high-power switching. To investigate its potential, we have undertaken gate switching at 100 kHz and a 10 percent duty cycle, using a constant drain bias of 10 V. These measurements reveal a near-ideal pulsed current across the entire temperature range (see Figure 5).

We have also examined whether there is any evidence for the formation of a virtual gate. This is not wanted, as it could lead to current collapse under pulsing. The good news is that there is only a very slight reduction in pulsed current at high gate voltages, indicating that a virtual gate is clearly not forming.

Given the success of GaN devices in the RF domain, it is natural to wonder whether our transistors could have an impact there. But before diving into this, it is essential to consider the electron mobility in the AlGaN HEMT. The concern is that moving to a channel with a ternary alloy will result in a large increase in alloy scattering. This could be particularly significant in aluminium-rich AlGaN, as polar optical phonon scattering effects will become stronger, because the Al-N bond has a greater difference in electronegativities than the Ga-N bond. At low and moderate temperatures, alloy scattering will be the limiting factor, but it will be overtaken by polar optical phonon scattering at elevated temperatures.

History attests to a lag between success in the DC domain and that in the RF. After the demonstration of the first ever GaN device in 1993, it took another three years to realise the first RF performance

We have modelled these two key effects and compared them with experimental values for mobility (see Figure 6). At room temperature, the channel mobility of the 85/70 device is just 310 cm^2 V^{-1} s^{-1}. This value, much lower than a GaN HEMT, results from the combination of alloy scattering and polar optical phonon scattering.

History attests to a lag between success in the DC domain and that in the RF. After the demonstration of the first ever GaN device in 1993, it took another three years to realise the first RF performance. With AlGaN channel HEMTs, the wait has been even longer – a HEMT with an AlGaN channel was first demonstrated in 2007, only within the last year have several RF results been published, including the efforts of our team.

Initial results produced by our 85/70 devices include an f_t of 28.4 GHz and an f_{max} of 18.5 GHz. Large-signal RF testing, performed at 3 GHz using a drain-source bias of 20 V and gate-source voltage of 3.75 V, reveals a peak output power of 15.8 dBm at a power-added efficiency of 11 percent.

Don't be surprised that these results are nowhere near those of today's GaN RF devices. After all, advanced techniques for RF device processing have not been used. It's also important to note that RF solutions for extreme environments do not exist today for GaN or SiC RF devices.

We would expect that as an awareness of the capability of the AlGaN HEMTs grows, and more reports emerge, there will be further development and additional improvements. In turn, more groups will get involved, collective knowledge will increase, and this will lead to additional breakthroughs.

Even in its infancy, it is clear that the AlGaN HEMT has the potential to complement its GaN cousin. Intrinsic mobility limitations will impact some applications in power switching, but there are new opportunities for this material system in extreme environments. Unlike other ultra-wide bandgap materials, developers of AlGaN HEMTs can draw on the breakthroughs made with a similar material system – the successes that have been accomplished during thirty years of investigating GaN – and accelerate the development and commercialisation of this very promising transistor.

This work was supported by the Laboratory Directed Research and Development program at Sandia National Laboratories. Sandia National Laboratories is a multi-program laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC (NTESS), a wholly owned subsidiary of Honeywell Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525. The views expressed in the article do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

Further reading

M. J. Martinez *et al*. IEEE Trans Nucl. Sci **66** 344 (2019)
P. H. Carey *et al.* IEEE JEDS **7** (2019)
A. G. Baca *et al*. ECS J. Solid State Sci. Technol. **6** Q161-Q165 (2017)

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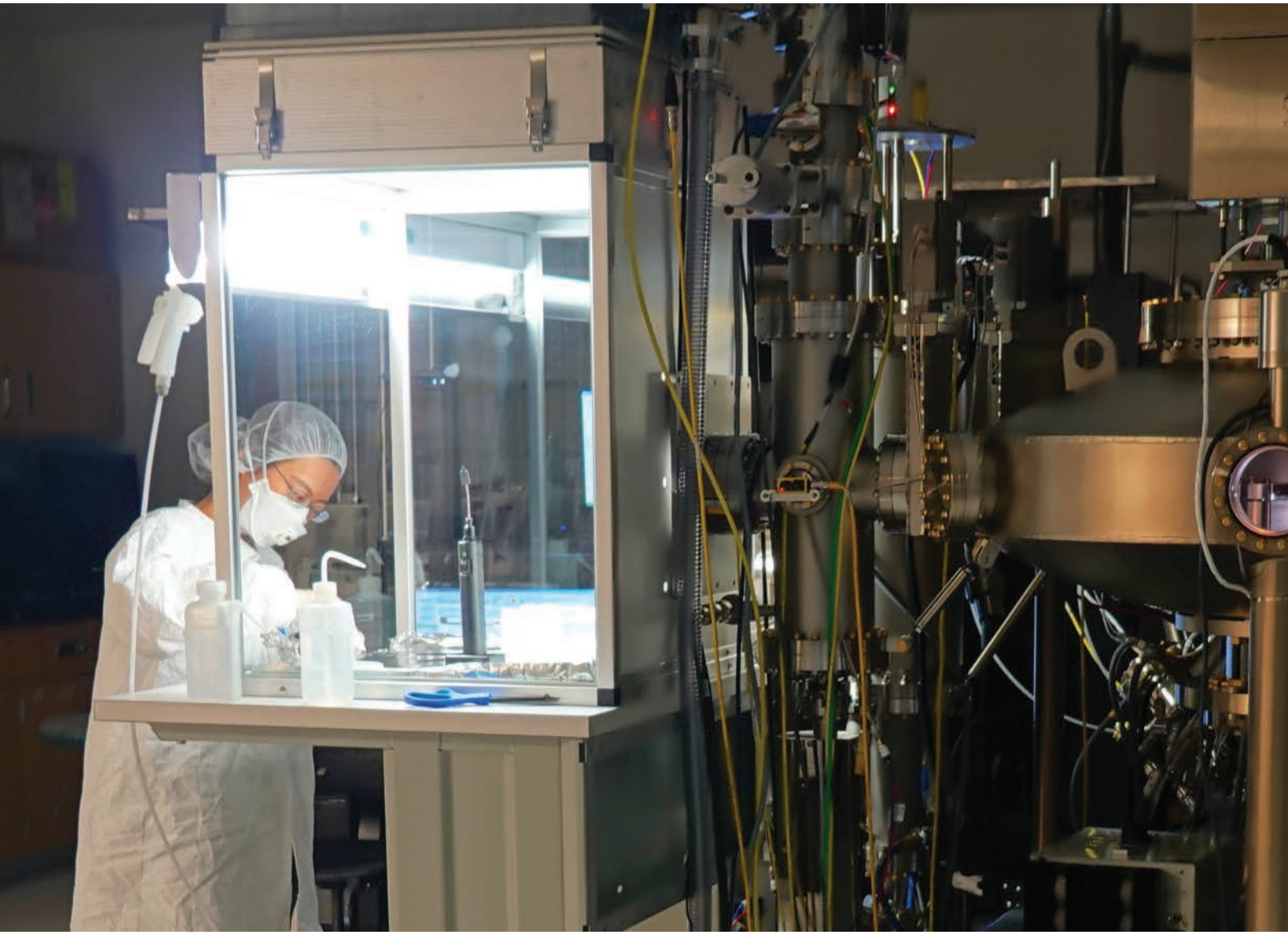
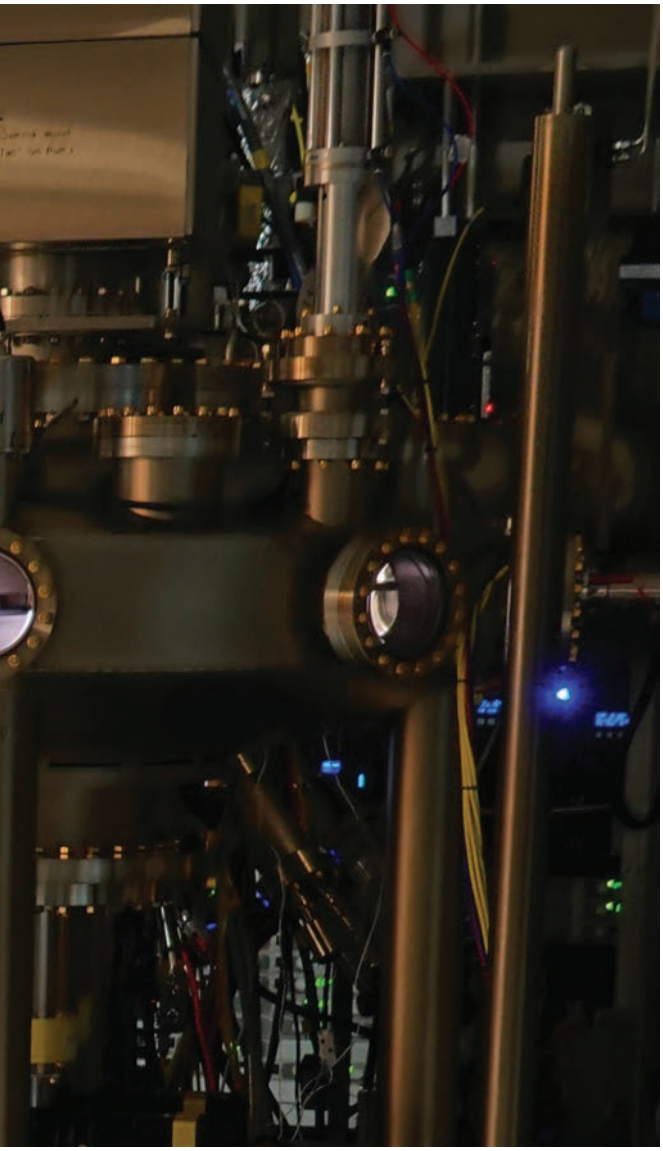


Extending the reach of photonic power

High-voltage photonic power converters designed for telecom wavelengths promise to extend the reach of power-over-fibre systems

BY MEGHAN BEATTIE AND KARIN HINZER FROM THE UNIVERSITY OF OTTAWA



Left: Molecular beam epitaxy at the University of Waterloo.

WE LIVE IN an increasingly interconnected world, depending heavily on electronic devices such as sensing and communications equipment. Delivering reliable power to these devices as they are deployed in more remote and extreme environments can be challenging. The conventional approach is to provide power over copper wire, but this is highly sensitive to electromagnetic interference and prone to heating and sparking in hazardous conditions. An alternative solution to these challenges is photonic power transmission. This involves a light source and a photonic power converter, which converts the light back into electricity.

Merits of the optical approach include full electrical isolation and immunity from electromagnetic interference. In addition, fibre is lighter and cheaper than copper cabling; it is more tolerant of the environment; and there is the potential for simultaneous power and data transmission using existing telecommunications technology.

The superiority of optical fibre for data transfer is well known in the telecommunications industry; however, there are still roadblocks to widespread implementation of photonic power transmission. In particular, long distance transmission remains a challenge – one that we are addressing in our research at the University of Ottawa with a novel chip design, operating at telecom wavelengths, that will offer tremendous improvement in the reach of power-over-fibre systems.

The light source for a photonic power transmission system can be either a laser or an LED. After transmission, light is transformed back into electrical power by a photonic power converter, also known as an optical power converter, photovoltaic power converter, laser power converter, or phototransducer. Optical power can be transmitted through free space, but it is usually preferable to route it through an optical fibre, which guides the light and eliminates the need for line-of-sight trajectories.

Just like solar cells, photonic power converters generate electrical power from light through the photovoltaic effect. When light impinges on the device, photons are absorbed, generating a potential difference, or photovoltage, and an electric current. However, photonic power converters have a key difference to solar cells – rather than being designed to generate as much power as possible from the very broad solar spectrum, which spans the ultraviolet to the infrared, they operate within a very narrow energy range that corresponds to the output of a laser or LED. This distinction allows photonic power converters to operate at efficiencies of up to 70 percent, much higher than a solar cell.

Photonic power has already been adopted in niche applications, powering sensors for high-voltage transmission-line monitoring and deployed in magnetic resonance imaging machines where strong magnetic fields prevent the use of copper wires.

The use of photonic power transmission is sure to grow – budding applications are numerous and varied. It is a promising option for providing power to sensors and smart electronics in autonomous vehicles, which require isolation in an electrically noisy environment. Opportunities also exist in emerging smart-grid infrastructures, which rely on vast arrays of sensors and inter-device communications, often operating in challenging environments with high voltages, electromagnetic interference and harsh weather. Other industries in which photonic power supply could make a positive impact are aerospace, avionics, defence, medicine, and telecommunications.

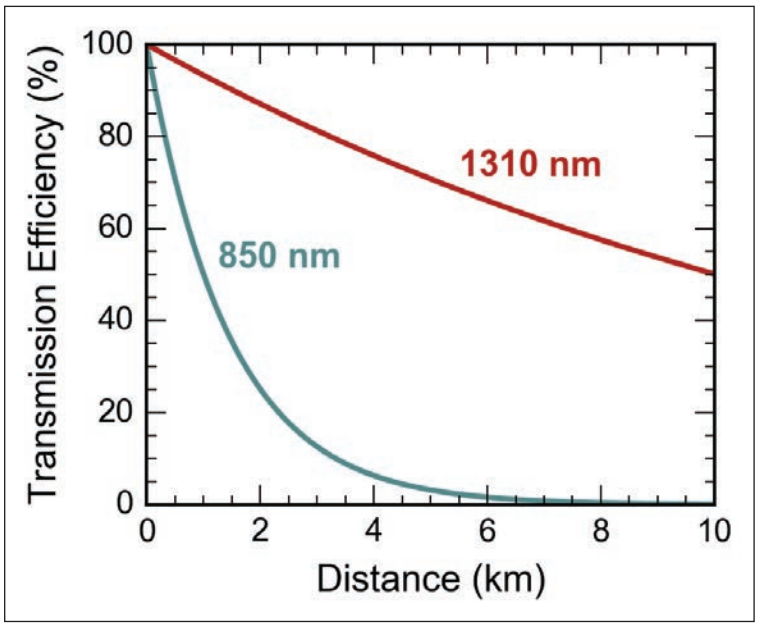


Figure 1. Optical fibre transmission efficiency as a function of distance for 850 nm and 1310 nm light. Attenuation coefficients are assumed to be 3 dB/km for 850 nm and 0.3 dB/km for 1310 nm.

Increasing the distance

As the majority of photonic power converters are based on GaAs, their absorption lies in the 850 nm band. That's far from ideal, because at this wavelength the optical attenuation in the fibre is around 3 dB/km – or, put another way, power halves for every kilometre it travels through the fibre. This restricts GaAs-based photonic power converters to operate in either free-space configurations, or in scenarios involving short fibre links (see Figure 1).

A far better option for power transmission over long lengths of fibre is to shift to a wavelength where attenuation is minimised. Opportunities exist in the O-band and C-band, found at 1310 nm and 1550 nm, respectively (see Figure 1 to appreciate the extent of the improvement). However, to make this adjustment, there must be a move from a GaAs-based material system to one such as InP, on which smaller bandgap absorbers can be grown.

Our team at the University of Ottawa is adopting this approach. We are developing the first vertical-segmented InP-based photonic power converters for operation at 1310 nm. To produce these devices, we are collaborating with a team at the University of Waterloo that uses MBE to make our epistructures. Grown on an InP substrate, these heterostructures feature a lattice-matched InAlGaAs absorber.

The move to 1310 nm slashes the attenuation in the fibre to just 0.3 dB/km, or 7 percent per kilometre, opening the door to power transfer over several kilometres. There is also the tantalising prospect of using the longer wavelength C-band for data transfer,

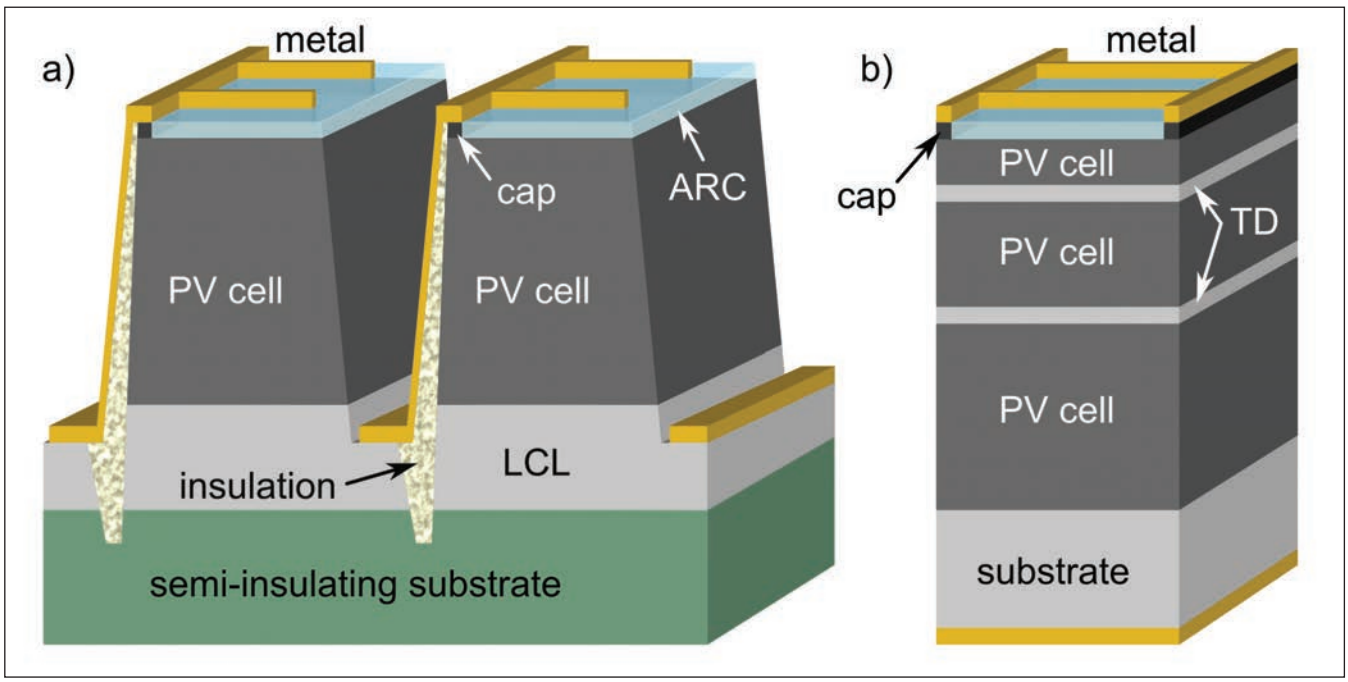


Figure 2. Typical design for a (a) lateral- and (b) vertical-segmented photonic power converter. ARC: antireflection coating, LCL: lateral conduction layer, PV: photovoltaic, TD: tunnel diode.

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Wavelength	Material	Segmentation	Voltage	Efficiency	Source
850 nm	GaAs	Vertical	6 V	70%	Broadcom / uOttawa
850 nm	GaAs	Vertical	23 V	60%	
9XX nm	Si	Lateral*	3 V	41%	MH GoPower
9XX nm	Si	Lateral*	20 V	40%	

Table 1. Record segmented photonic power converter efficiencies at various wavelengths and operating voltages. *MH GoPower photonic power converters are multi-junction, but illuminated from the side so that they retain the same requirements for precise alignment and uniform illumination as standard lateral designs.

enabling a single fibre to simultaneously provide power transfer and communication.

Boosting the voltage

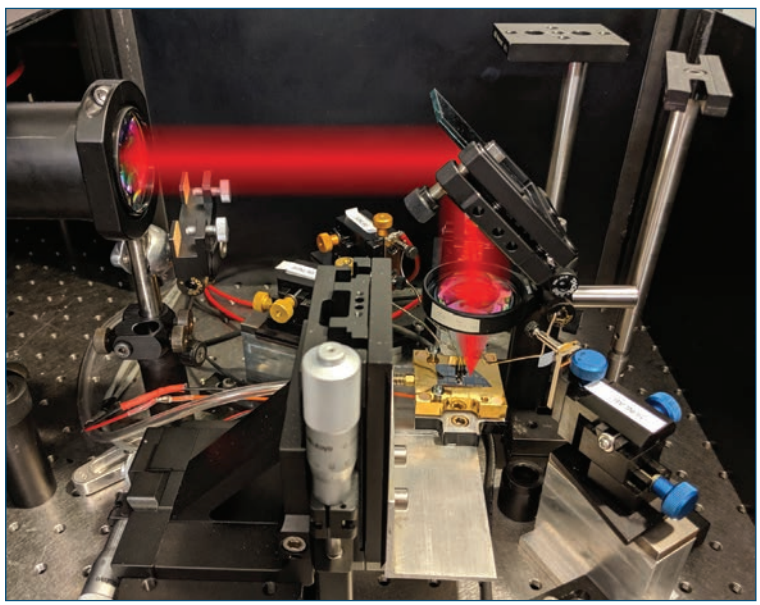
The operating voltage of a photonic power converter is limited by the bandgap of its light-absorbing region. GaAs-based devices, grown either by MBE or MOCVD, generate about 1.2 V, which is insufficient for most power applications. Conventional DC-to-DC converters could boost this voltage. However, a far better option for ensuring immunity to electromagnetic interference is to scale the voltage within the device itself, using series connections.

One widely used option is to form laterally segmented, interconnected devices (see Figure 2(a)) to generate output voltages of up to 20 V. This voltage is high enough to ensure that devices can be powered directly from the photonic power converter. However, this approach requires complex fabrication, and the devices that result are impaired by the strict requirement for precise alignment and uniform illumination across all segments. If one segment receives less illumination, it produces less photocurrent, limiting the current of the entire device and reducing its output power. Practical efficiencies for this type of device are typically 30 percent to 35 percent, although efficiencies under ideal conditions have hit the mid-50 percent range.

Due to these drawbacks, state-of-the-art photonic power converters rely on vertical interconnections, similar to multi-junction solar cell technology (see Figure 2(b)). The absorbing material is portioned into optically thin segments, series-connected with tunnel diodes. With this type of architecture, high output voltages are combined with high efficiencies. For example, a 20-junction GaAs device made by Broadcom Semiconductors ULC (formerly Azastra Opto) can produce an output voltage of 23 V. Fabrication is straightforward, and devices have good tolerance to non-uniform illumination, enabling efficiencies in excess of 60 percent. The record for efficiency, realised by Broadcom in partnership with our team, is as high as 70 percent for a five-junction device (see Table 1 for a brief overview of record efficiencies for segmented photonic power converters).

To boost the voltage of our 1310 nm photonic power converters, we employ this state-of-the-art, vertical-segmented, multi-junction design. The InAlGaAs absorbing region with a bandgap of 0.864 eV is partitioned into semi-transparent photovoltaic sub-cells. By precisely tuning the thickness of each layer, we ensure that each vertical segment generates the same current. This is accomplished with the thinnest layer at the top and the thickest at the bottom. The total thickness of the absorbing layers is almost 5 μm, ensuring at least 98 percent absorbance of incoming light. By shifting the composition of the quaternary, we can produce transparent lattice-matched tunnel diodes between each sub-cell. Ultimately, high-quality, vertical-segmented photonic power converters will be achieved.

We have produced a range of single-junction photonic power converters to determine the relationship between thickness of the absorber and quantum efficiency (see Figure 3). For these test devices, we have selected layers with thicknesses that would



Experimental setup to measure current-voltage characteristics for photonic power converters with overlay of beam path.

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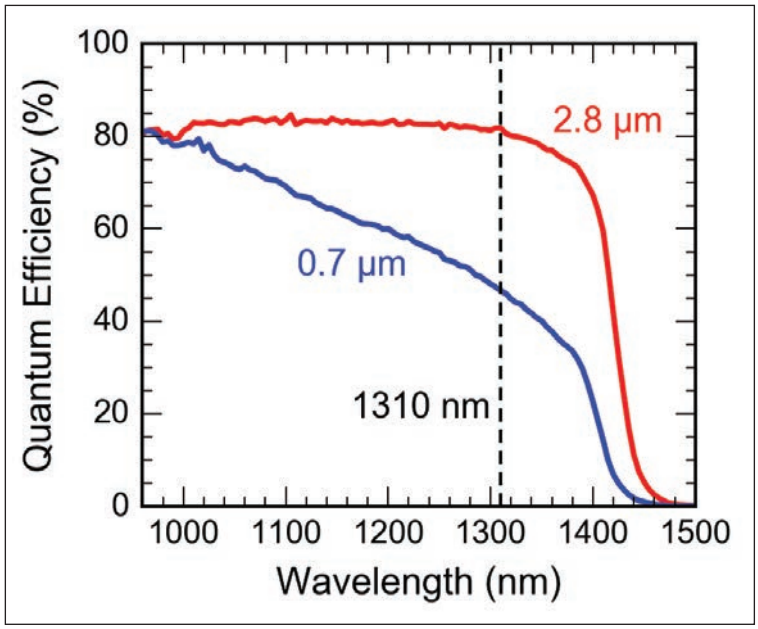


Figure 3. Quantum efficiency of optically thin, 1310 nm single-junction photonic power converters of varying thickness, designed to be incorporated into a multi-junction stack.

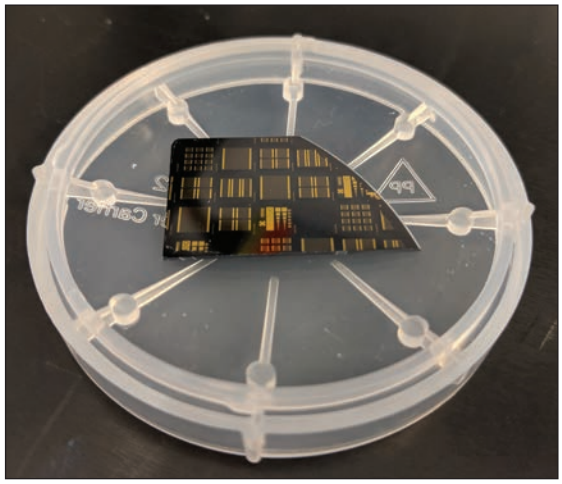


Figure 4. Single-junction photonic power converter chips for O-band operation.

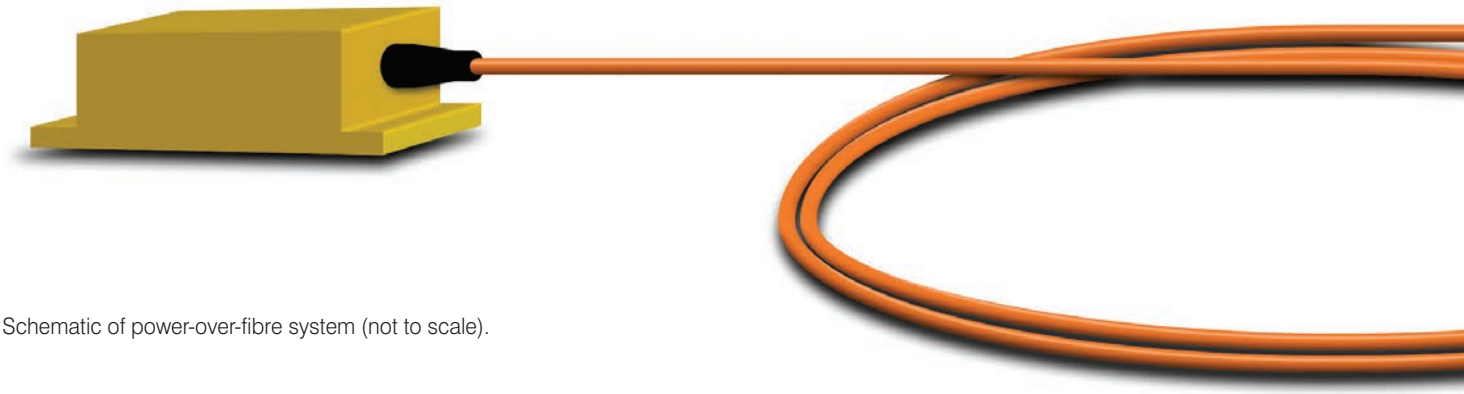
be used in a multi-junction structure. As expected, thicker layers increase absorbance, and by extension, quantum efficiency.

One of our current activities is to establish an in-house fabrication process for device testing (see Figure 4 for a partially fabricated, single-junction photonic power converter wafer). Development of a complete multi-junction structure is also underway.

To benchmark the performance of our devices, we use the detailed balance limit. This represents the theoretical limiting efficiency of the device, and assumes that every absorbed photon generates a single electron-hole pair, completely separated and perfectly conducted. Calculations are carried out in the radiative limit, so excited charges can only relax by radiating light that may be reabsorbed in the device. These calculations offer an upper limit on what can be realised, as real devices are impaired by imperfect absorption and conduction, as well as non-radiative forms of charge relaxation. As we improve material quality, the performance of our devices gets closer to the limiting efficiency.

For our design, the theoretical voltage per junction is 0.63 V, in the radiative limit for an input power density of 10 W cm^{-2}. Based on these results, an ideal 10-junction photonic power converter of our design could achieve an output voltage over 6 V, and a limiting efficiency of 65 percent. For realistic material, a 10-junction photonic power converter should power a 5 V device with an efficiency of between 50 percent and 60 percent. Cranking up the input power, the current will increase linearly and voltage logarithmically. These changes would push the limiting efficiency to over 70 percent in the radiative limit for 100 W cm^{-2}.

Further improvements in the voltage and the efficiency will result from moving to a slightly larger bandgap for the absorbing region, aligning the absorption edge to the incoming light at 1310 nm – which corresponds to a photon energy of 0.95 eV – and thereby reducing the amount of energy lost to heat. Note that maintaining absorbance at 98 percent requires the use of a thicker absorber.



Schematic of power-over-fibre system (not to scale).

Wavelength	Material	Distance	Transmission Efficiency	Combined Fiber-PPC Efficiency*
850 nm	GaAs	1 km	50%	30%
		10 km	0.1%	0.06%
1310 nm	InAlGaAs/InP	1 km	93%	56%
		10 km	50%	30%

Table 2. Estimated efficiencies for power-over-fibre systems assuming 60 percent photonic power converter efficiency. *Does not account for efficiency of the light source (laser or LED).

Possibilities and challenges

With our design of photonic power converter, we expect to transmit 1310 nm photonic power over a 1 km length of optical fibre with a 56 percent efficiency. That's nearly a two-fold increase over a comparable GaAs-based 850 nm system. The performance provided by our 1310 nm link paves the way to powering 5G devices within the internet-of-things. Even for distances as long as 10 km, we expect 30 percent efficiency, a tremendous improvement over GaAs-based devices, which can only realise a 0.06 percent efficiency (see Table 2 for a summary of estimated efficiencies).

Within a full power-over-fiber system, the overall electrical-optical-electrical efficiency is not just determined by the efficiency of the photonic power converter and the extent of fibre attenuation, but also by the efficiency of the light source. For high-power lasers operating at 1310 nm, efficiencies can reach the mid-30 percent range. Assume an electrical-optical conversion efficiency of 35 percent, and a photonic power converter efficiency of 60 percent, and the electrical-optical-electrical efficiency can be as high as 21 percent through free space. Add in 1 km and 10 km lengths of fibre, and the total efficiency will drop to 20 percent and 11 percent, respectively, assuming perfect optical coupling.

These efficiencies indicate that fully optical power-over-fibre systems could be deployed over distances up to 10 km, delivering reasonable performance and enabling reliable, fully isolated power supply to hazardous environments. Crucially, this power transfer technology could be added to existing fibre networks, previously reserved for data transfer, by introducing a 1310 nm light source and a photonic power converter.

Our efforts, and those of our peers, are expanding the versatility of power-over-fibre systems. As the reach of photonic power extends, the catalogue of applications will continue to grow. There is no doubt that this technology has a very bright future.

Further reading

D. Xia *et al*. "Opportunities for High Efficiency Monochromatic Photovoltaic Power Conversion at 1310 nm," 46th IEEE PVSC, June 2019

M. Wilkins *et al.* IEEE Trans. Power Electron. **34** 1054 (2019)

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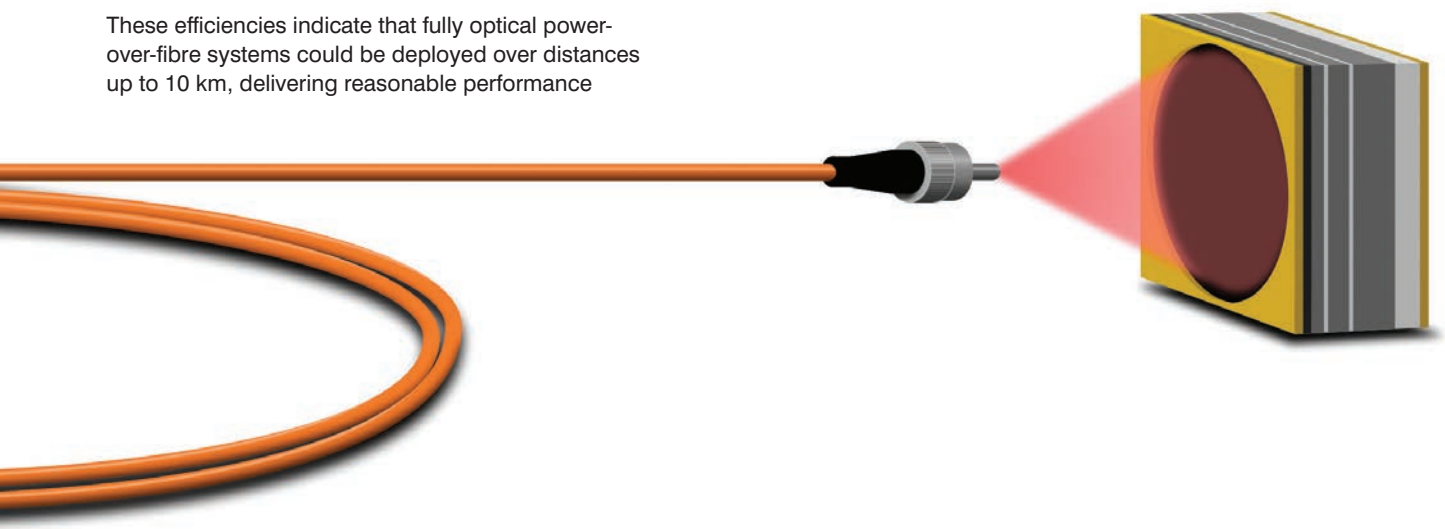

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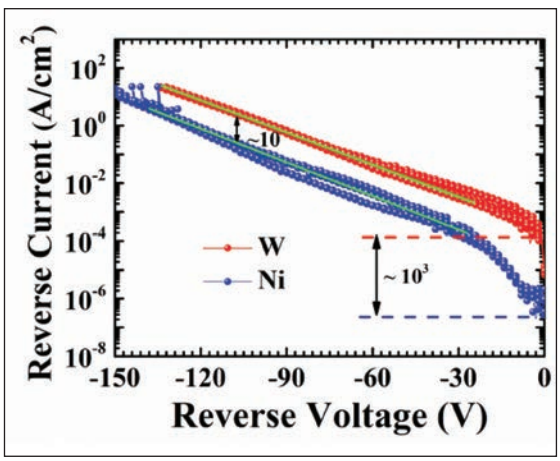
Tungsten contact improves GaN diodes

Replacing conventional contacts in GaN Schottky barrier diodes with those made from tungsten trims the turn-on voltage

INTRODUCING a tungsten contact has enabled researchers at Xidian University, China, to improve the performance of GaN Schottky barrier diodes with a vertical geometry. The engineers claim that the tungsten anode has led to a new low for the turn-on voltage, for variants of this class of diode with a breakdown voltage of 100 V or more.

Spokesman for the engineers, Shenglei Zhao, believes that another important aspect of the team's work is the identification of the reverse leakage current mechanism. It is argued that as the reverse bias increases, the dominant leakage mechanism shifts from thermionic emission to variable range hopping.

All those recent findings came from making and studying quasi-vertical GaN Schottky barrier diodes, which are a class of device that is normally fabricated on silicon or sapphire and features both the anode and the cathode on its front side. In contrast, fully-vertical devices are made on GaN substrates, and have one contact on either side.



As the reverse bias increases, the dominating mechanism for the leakage current switches from thermionic emission to variable range hopping.

According to Zhao, compared with their fully vertical cousins, two downsides of quasi-vertical devices are a larger active area and a higher specific on-resistance. These deficiencies stem from the front-side cathode.

Weighed against these drawbacks are several strengths of the quasi-vertical design. "The cost of sapphire and silicon substrates is much lower than that of the GaN substrates," says Zhao, who points out that it is also easier to fabricate quasi-vertical devices on large scale wafers; and with both electrodes on the same side, this architecture is suitable for designing and making monolithic power ICs.

Fabrication of the GaN quasi-vertical Schottky barrier diodes begins by loading sapphire substrates into an MOCVD chamber, and growing a 2 μm-thick undoped layer of GaN, followed by a 3.5 μm-thick heavily doped layer of GaN and finally a lightly-doped 1.3 μm-thick layer of GaN. Subsequent mesa etching accesses the heavily-doped layer, before electron-beam evaporation adds a Ti/Al/Ni/Au ohmic contact, improved by rapid thermal annealing under nitrogen gas. Completion of the device involves sputtering, to form a Schottky electrode. It has a diameter of 76 μm, and is made from 50 nm-thick tungsten, followed by 150 nm of gold.

For comparison, the researchers produced an identical device, aside from the electrode. The control has a conventional electrode, comprising 45 nm-thick nickel and 150 nm-thick gold. Current-voltage measurements on 20 diodes, half with a tungsten anode and half with one made from nickel, reveal that both types of device have good uniformity.

Ideality factors, extracted from these plots, are 1.01 for diodes with the tungsten anode, and 1.02 for the nickel variant. According to the team, these nearly ideal characteristics indicate that the interface of the Schottky contact is highly homogeneous, and the current is dominated by thermionic emission.

Switching from the conventional nickel contact to one made from tungsten trims the turn-on voltage from 0.60 eV to 0.39 eV, but degrades the on-off ratio – it falls from 10^{10} to 10^8.

Under zero bias, the researchers find that thermionic emission dominates the leakage current. It is three orders of magnitude higher in the diodes with a tungsten anode, due to the lower Schottky barrier height. Crank up the reverse bias, and the difference in leakage current drops to just one order of magnitude. This occurs because variable range hopping takes over as the dominate leakage mechanism.

The team goals for the future include optimising GaN epitaxy, in order to increase the breakdown voltage to more than 1 kV while maintaining a low turn-on voltage. "Several other anode metals will be compared to pursue a better trade-off between turn-on voltage and leakage current," says Zhao.

Reference

Z. Bian *et al.* Appl. Phys. Express **12** 084004 (2019)

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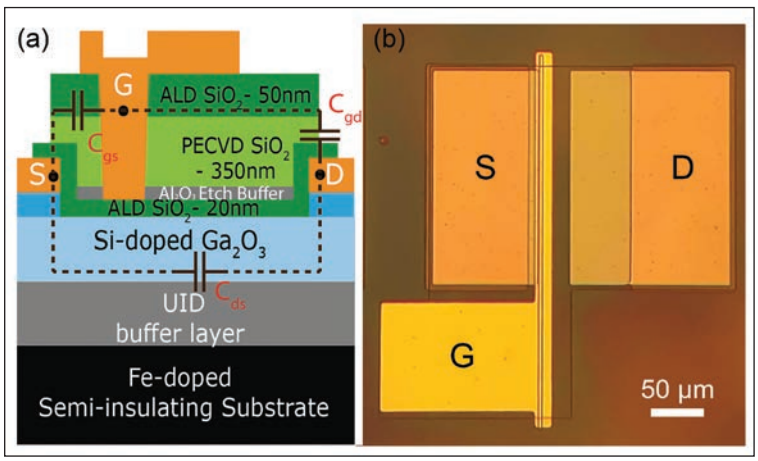
Slashing the on-resistance of high-voltage Ga_2O_3 MOSFETs

Field-plated gallium oxide MOSFETs combine a high breakdown voltage with a low on-resistance

GALLIUM OXIDE TRANSISTORS have great potential, promising to combine incredibly high breakdown voltages with high current densities and high operating temperatures.

Delivering on all these fronts is very challenging, as spin-on-glass and ion-implantation techniques used to form source and drain contacts require high-temperature annealing processes that can introduce defects into the material. But success is possible by turning to MBE to grow a highly doped capping layer on top of the channel, according to recent work by a team of engineers at the University of Buffalo.



The structure of the Ga_2O_3 low-resistance, high-voltage HEMT (a), and an optical image of the fabricated device (b).

These researchers have been developing Ga_2O_3 MOSFETs for several years, with efforts initially focused on increasing the breakdown voltage. In 2018 the team triumphed, propelling the record for breakdown voltage from 750 V to 1850 V. The new benchmark, produced with a device with a gate length of 20 µm, resulted from introducing a field plate, alongside the addition of Flourinert around the transistor to prevent air breakdown.

Unfortunately, these devices had a very high on-resistance, stemming from variability in the high-temperature spin-on-glass process used to create the source and drain contacts. Now this weakness has been addressed, without compromising the breakdown voltage, by switching to an MBE step. This allows the two contacts to be formed at a far lower temperature.

Fabrication of the MOSFETs began by loading 500 µm-thick, iron-doped semi-insulating Ga_2O_3 substrates into an ozone-MBE chamber and growing a stack of epitaxial layers. A 200 nm-thick unintentionally doped layer of Ga_2O_3 that prevents diffusion of iron is deposited first, followed by a 200 nm-thick silicon-doped channel and a 30 nm-thick caping layer, grown for the ohmic contact.

Electron beam evaporation added Ti/Au/Ni source and drain contacts, with contact resistance reduced by rapid thermal annealing at 520 °C. Reactive ion etching removed the capping layer, and then provided device mesa isolation. UV ozone treatment followed, before deposition of the gate oxide.

The oxide is deposited by ALD, followed by PECVD. According to team spokesman Ke Zeng, ALD is used to enhance the top layer oxide strength, because it provides a denser, higher-quality film. Measurements on the MOSFETs revealed an output current of 20 mA mm^{-1} and an on-resistance of 520 mΩ cm^2. The sub-threshold swing at 10^{-6} mA mm^{-1} is 1.5 V dec^{-1}, indicating that the interface state density is 2.8 x 10^{13} cm^{-2} eV.

Although the team have reduced the on-resistance, it is still larger than the best values reported by other groups. Zeng and co-workers believe that this could be due to lower doping in the channel, the depletion of the source access region, and the high interface state density.

Zeng says that he and his co-workers have always struggled on the interface trap problem, simply because they have not had enough time and man-power to tackle this issue.

However, he believe this issue can tackled by using some form of surface treatment prior to gate oxide deposition. Options include aggressive wet chemical cleaning and reactive-ion etching, tuned to smoothen the surface.

Zeng believes that the breakdown voltage of the team's MOSFETs can be higher, and their on-resistance lower, by implementing new device structures and special treatment techniques.

Reference

K Zeng *et al.* Appl. Phys Express **12** 081003 (2019)

Realising single-mode operation in GaN VCSELs

GaN VCSELs with curved mirrors produce the first single transverse-mode operation

RESEARCHERS from Sony are claiming to have broken new ground by fabricating the first GaN VCSELs with single transverse-mode operation.

Their devices, emitting at around 443 nm, are not the first form of VCSEL to operate in this manner. Even before the turn of the millennium, GaAs VCSELs were operating with single transverse-mode operation. However, in GaAs VCSELs this is accomplished by reducing the current aperture to around just 3 μm to prevent higher order modes from being excited. This holds back the output power – for the common emission wavelength, 850 nm, it is typically no more than 3 mW.

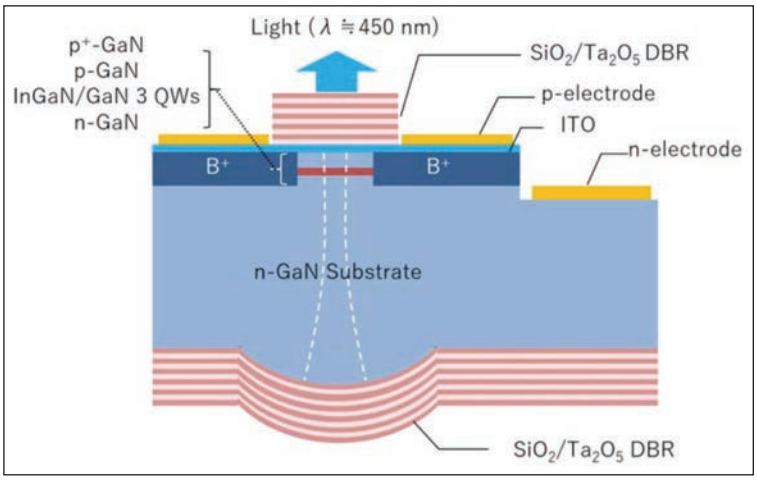
Sony's design overcomes this limitation. The bottom planar mirror is replaced with one that is curved, a change that can enhance optical confinement. What's more, the new architecture allows the VCSEL to incorporate a larger cavity, aiding optical confinement.

The team from Japan have produced a portfolio of GaN VCSELs, featuring different mirror curvatures and a range of diameters for the current aperture.

Fabricating the devices began by loading an *n*-type GaN substrate into an MOCVD chamber, and depositing an epitaxial stack that consists of a layer of *n*-type GaN, an active region with three InGaN quantum wells, and a layer of *p*-type GaN. Vacuum deposition followed, adding a layer of indium tin oxide, followed by a top-side distributed Bragg reflector (DBR), made from seven pairs of Ta_2O_5 and SiO_2. Note that the number of layers in this DBR is less than that it is in previous VCSELs made by Sony, in order to enhance extraction efficiency.

The engineers used boron-ion implantation to form current apertures with diameters ranging from 3 μm to 8 μm. After selective reactive-ion etching down to both the ITO and the *n*-type GaN, a pair of metal contacts were added, made from a Ti/Pt/Au stack. Contacts connected to the ITO and *n*-type GaN created current paths for injecting holes and electrons, respectively.

Prior to the formation of the curved mirror, the backside of the substrate was polished down to a thickness of 20 μm. Then, ball-up resin patterns were added, acting as sacrificial masks during subsequent reactive-ion etching, which creates a curved surface. Finally, vacuum deposition added 14 pairs of Ta_2O_5 and SiO_2, to create a bottom DBR.



Sony's VCSEL design, featuring a curved bottom mirror, enables this class of device to deliver single transverse mode operation.

Sony's engineers measured the emission characteristics of a range of VCSELs, mounted with a *p*-side up configuration in TO5.6 packages. These lasers were operated in continuous wave-mode at 20 °C.

Studies on the VCSELs with a bottom mirror with a radius of curvature of 51 μm revealed numerous peaks, associated with higher-order transverse modes, in the emission spectra of devices with a current aperture of 6 μm. Reducing the aperture diameter to 5 μm and then on to 4 μm led the strength of these higher order modes diminish again and again – and when this aperture was just 3 μm across, only peaks associated with the longitudinal mode existed.

The researchers have also scrutinised the emission from a pair of VCSEL with differing radii of curvature, but the same diameter of current apertures – it is 4 μm. For the variant with a 31 μm radius of curvature, multiple peaks are observed in the emission spectrum and the far-field pattern, implying multi-mode transverse operation. In stark contracts, for the VCSEL with a 51 μm radius of curvature, Gaussian-like profiles were seen in the far-field for currents up to 6 mA. Based on these results, the team concluded that the radius of curvature of the mirror can control single transverse-mode operation.

Driven at 6 mA, this VCSEL emitted an output power of 3.2 mW, and had a side-mode suppression ratio of 30 dB.

Reference

H. Nakajima *et al.* Appl Phys. Express **12** 084003 (2019)

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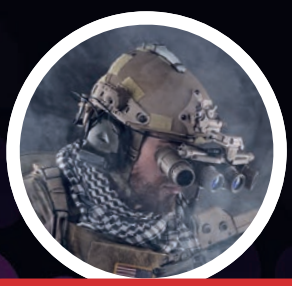

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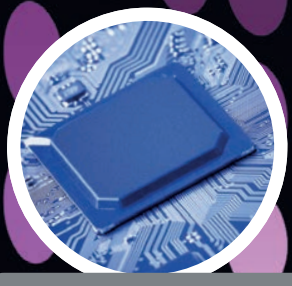

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